Simultaneous Switching Considerations

1987

Design Considerations

TEXAS
INSTRUMENTS

Simultaneous Switching Considerations

Scott Abramson
Charles Hefner
Dan Powers

TEXAS
INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes in the devices or the device specifications identified in this publication without notice. TI advises its customers to obtain the latest version of device specifications to verify, before placing orders, that the information being relied upon by the customer is current.

TI warrants performance of its semiconductor products to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems such testing necessary to support this warranty. Unless mandated by government requirements, specific testing of all parameters of each device is not necessarily performed.

In the absence of written agreement to the contrary, TI assumes no liability for TI applications assistance, customer's product design, or infringement of patents or copyrights of third parties by or arising from use of semiconductor devices described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor devices might be or are used.

Contents

List of Illustrations

Abstract

This application report is presented to provide an understanding of the potential problems of multiple outputs switching and to develop a standardized methodology for the evaluation of simultaneous switching. The effects of simultaneously switching outputs on a multiple output device are examined from a historical point of reference as well as from a first order theoretical evaluation of the phenomena. The impact of several system parameters are evaluated for their effect upon the simultaneous switching performance of a CMOS logic device. A standardized test methodology for the evaluation of simultaneous switching effects is presented in Appendix A. Appendix B provides a parts and vendor list for Texas Instruments ACL characterization board. The results of this paper are presented to assist the end user of ACL (Advanced CMOS Logic) devices in evaluating simultaneous switching effects.

Introduction

TTL and CMOS logic devices have evolved with decreases in geometries, power dissipation, and propagation delay. This evolution has allowed the system designer to develop end equipment with more functionality per unit volume as well as systems that solve increasingly complex problems. The benefits resulting from this technological evolution have been accompanied with some undesired results. As logic devices have become faster, output edge rates have increased from 5 ns/V to 1 ns/V. These faster slew rates can amplify system problems such as reflections on transmission lines, crosstalk between adjacent signal paths, and power supply noise.

The system engineer skilled in the art of high-speed logic design is aware of the system implications of higher switching speeds as well as the effect of switching multiple outputs simultaneously on a single device. The consequences of simultaneous switching include self induced noise on inactive outputs, loss of data, and propagation delay degradation. These phenomena are found to some degree in all high-speed logic families. The 74ALS, 74F, and 74AS logic families were the first bipolar families in which simultaneous switching noise became a major issue. System design engineers developed techniques to deal with the levels of switching noise, typically 1.1 volt glitches for octal devices, generated by this class of product.

Historically, CMOS logic has been somewhat immune to this class of problems since "the state of the technology" limited output drive and propagation delays. With the introduction of sub 2 micron gate lengths, CMOS logic devices are now capable of propagation delays and output drive levels equivalent to advanced bipolar logic devices, such as 74ALS and 74F. These performance levels place Advanced CMOS Logic (ACL) in the high-speed logic arena and have caused significant simultaneous switching noise problems for end pin ACL devices. Figure 1 illustrates the level of simultaneous switching noise obtained for standard circuit design and packaging techniques.

1

ACTIVE OUTPUTS

V$_{OLP}$

INACTIVE OUTPUT

21.500 ns	46.500 ns	71.500 ns

Time — ns

Ch.1 = 1.000 V/div
Ch.2 = 1.000 V/div
Timebase = 5.00 ns/div
Vmarker1 = −1.820 V

Vmarker2 = 2.400 V

Offset = 2.000 V
Offset = 2.000 V
Delay = 46.500 ns
Delta V = 4.220 V

7 outputs switching, 1 low
V$_{CC}$ = 5 V, T$_A$ = 25 °C
V$_{IN}$ = 20% − 80% rail
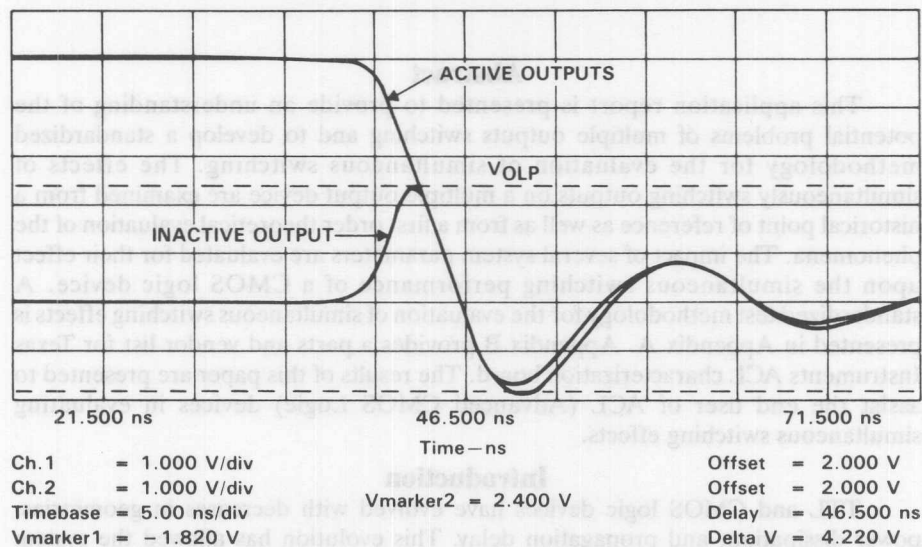
Figure 1. End-Pin Simultaneous Switching Noise Waveform

Simultaneous Switching Phenomenon

All CMOS logic devices operate by either charging or discharging capacitive loads. The load capacitor makes the instantaneous switching of logic levels impossible. This becomes apparent when one considers the MOS transistor has a finite "on" resistance through its conducting channel. Without the package parasitic inductance, an output structure for a single logic High to logic Low transition can be modeled as an RC network as shown in Figure 2.

The value of the resistor is determined by the size of the output transistor. EPIC™ (Enhanced Performance Implanted CMOS) ACL output structures are optimized to drive capacitive loads of 50 pF and transmission lines of impedances less than 50 Ω. Not only are these outputs designed to enhance ac switching performance for capacitive loads and low-impedance lines but they are designed to provide dc currents for CMOS and TTL loads. This optimization determines the output transistor sizing and yields values of channel resistance of 8 Ω to 12 Ω.

EPIC is a trademark of Texas Instruments Incorporated
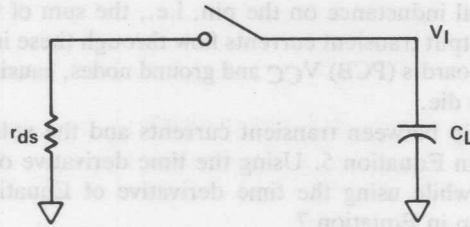
Figure 2. RC Model of a CMOS Output for the High-to-Low Transition

The current that flows in the circuit shown in Figure 2 can be modeled as Equation 1 which describes the relationship of current and voltage for a capacitor.

$$i = \frac{dq}{dt} = C\frac{dv}{dt} \tag{1}$$

Considering the on resistance of the MOS transistor as shown in Figure 2 and solving for the charging/discharging current, leads to the following relationship.

$$i = \frac{V_i}{r_{ds}} e^{-\frac{t}{r_{ds}C}} \tag{2}$$

where: r = on resistance of the transistor
C = load capacitance
V_i = initial voltage on the capacitor at time zero (typically a V_{OH} or V_{OL}.)

The current flow and the interaction of this current with package parasitic impedances are the determining factors in the performance degradation observed when several outputs are switched simultaneously on a multiple output device. The package parasitics that affect device performance to the largest extent are the self and mutual inductances associated with each package lead and bond wire. For a pair of simple parallel conductors, the values for self and mutual inductance can be obtained from Equations 3 and 4.[1] Through the remainder of this paper, the term inductance

$$L_i = \frac{\ell}{I} \int_o^\rho B_\theta \left(\frac{r}{\rho}\right)^2 dr = \frac{\mu\ell}{8\pi} \tag{3}$$

$$M = \frac{\wedge}{I} = 5\ell\left[\ell n\left(\frac{\ell}{d} + \sqrt{1+\left(\frac{\ell}{d}\right)^2}\right) - \sqrt{1+\left(\frac{d}{\ell}\right)^2} + \frac{d}{\ell}\right]nh \tag{4}$$

3

will refer to the total inductance on the pin, i.e., the sum of the self and mutual inductances. The output transient currents flow through these inductances between the Printed Circuit Board's (PCB) V_{CC} and ground nodes, causing inductive voltage spikes on the silicon die.

The relationship between transient currents and the voltage induced on an inductor is defined in Equation 5. Using the time derivative of i from Equation 1 yields Equation 6, while using the time derivative of Equation 2 generates the equivalent expression in Equation 7.

$$v_L = -L\frac{di}{dt} \tag{5}$$

$$v_L = -L\ C\frac{d^2V_i}{dt^2} \tag{6}$$

$$v_L = \frac{V_iL}{r_{ds}^2C}e^{-\frac{t}{r_{ds}C}} \tag{7}$$

where: v_L = voltage induced upon the silicon die
　　　　L = total inductance on the pin
　　　　r = on resistance of the transistor
　　　　C = load capacitance
　　　　Vi = initial voltage on the capacitor at time zero (typically a V_{OH} or V_{OL})
　d^2V/dt^2 = change in the slope of the transition edge

By inspection it can be seen the current that flows when N outputs are switched simultaneously is N times Equation 2. This relationship will hold true until the device begins to limit the transient current flow. As the above equations indicate, the induced voltage varies linearly with the total inductance on the pin. For this reason, the elimination of sockets and any other inductive components is required when using ACL devices. Texas Instruments has taken several steps to reduce the effects of simultaneous switching. In order to reduce the inductance term in Equations 5 through 7, Texas Instruments has introduced the EPIC™ ACL family in a center pin package. This packaging scheme reduces parasitic ground and power pin inductances by placing the ground and Vcc pins in the center of the package. Outputs are positioned around the ground pins to minimize the effective inductance of the outputs to ground and to provide a flow-through architecture. Texas Instruments has also introduced an innovative patent pending OEC™ (Output Edge Control) circuitry which essentially rounds off the upper and lower portions of the output edge while maintaining the rapid transition through the threshold region. The OEC™ is

OEC is a trademark of Texas Instruments Incorporated

composed of several small transistors which turn on or off in rapid succession. Rounding the upper and lower edges reduces the change in the slope of the output edge which directly reduces the induced voltage of Equation 6. For a more detailed description of the OEC circuitry see Texas Instruments application report "EPIC™ ACL Output Edge Control".

Texas Instruments has taken these measures to improve the reliability of systems utilizing ACL devices. The implementation of center pin power and ground along with the OEC™ reduces the noise due to simultaneous switching and therefore the effort required for a system designer to implement ACL. The voltage induced on a quiescent pin during simultaneous switching will be referred to as V_{OLP} or V_{OHV} throughout the remainder of this paper. V_{OLP} is defined as the maximum (peak) voltage induced on a quiescent low level output during switching of other outputs. VOHV is defined as the minimum (valley) voltage induced on a quiescent high level output during switching of other outputs. Figure 3 illustrates V_{OHV} and V_{OLP}.
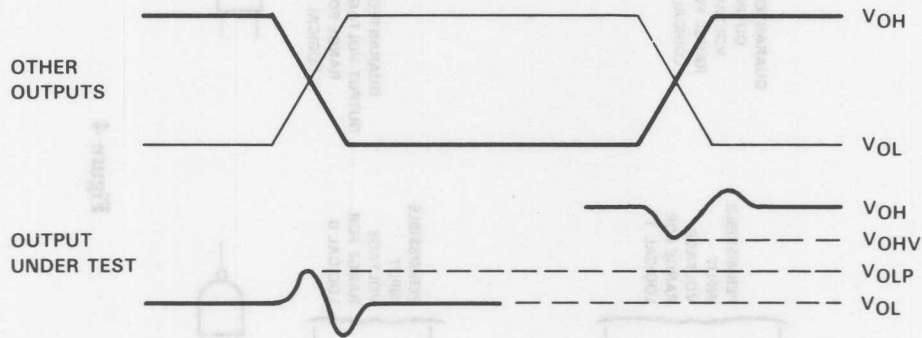
NOTES: A. V_{OHV} and V_{OLP} are measured with respect to ground reference near the output under test.
B. Input pulses have the following characteristics: PRR $\leq$ 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 1 ns.

Figure 3. Quiescent-Output Disturbance Voltage Waveforms

(a) TTL dc Noise Margin

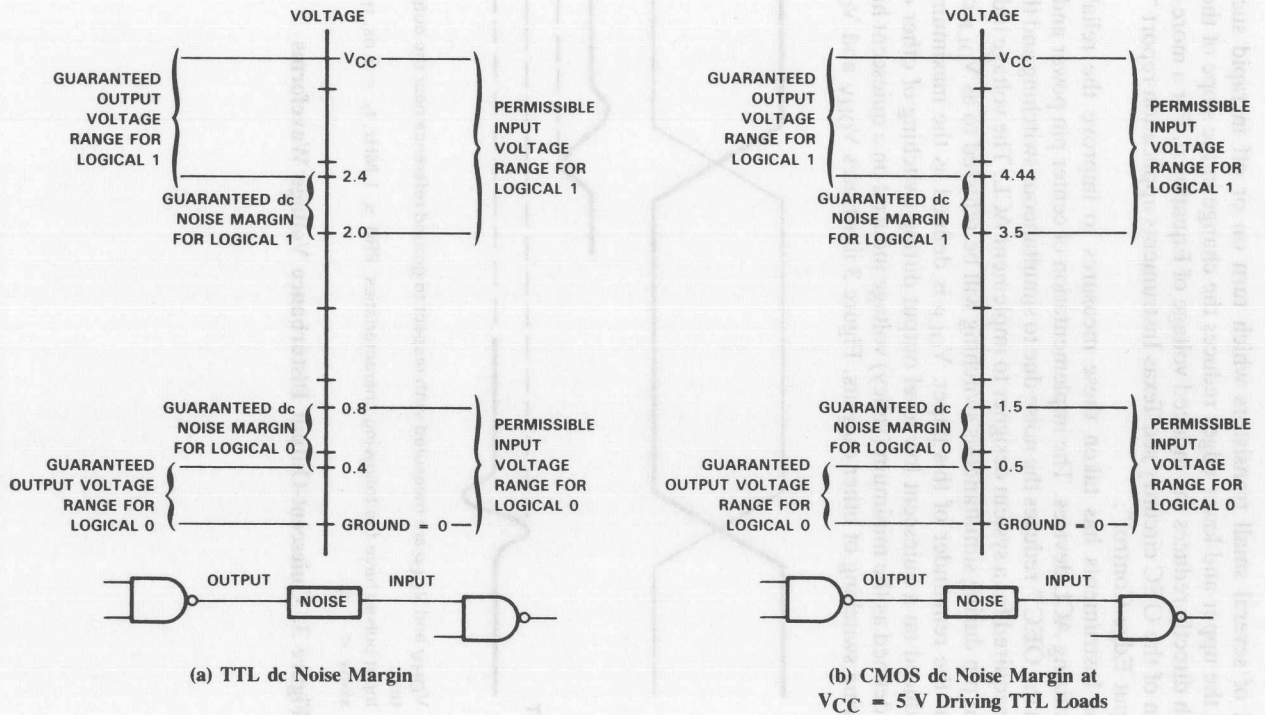**(b) CMOS dc Noise Margin at V_{CC} = 5 V Driving TTL Loads**
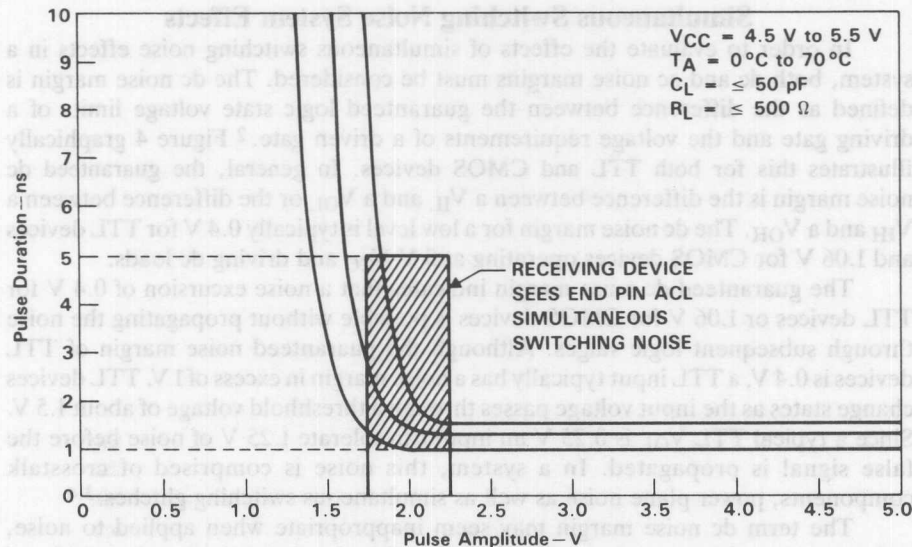
Figure 4

Simultaneous Switching Noise System Effects

In order to evaluate the effects of simultaneous switching noise effects in a system, both dc and ac noise margins must be considered. The dc noise margin is defined as the difference between the guaranteed logic state voltage limits of a driving gate and the voltage requirements of a driven gate. [2] Figure 4 graphically illustrates this for both TTL and CMOS devices. In general, the guaranteed dc noise margin is the difference between a V_{IL} and a V_{OL} or the difference between a V_{IH} and a V_{OH}. The dc noise margin for a low level is typically 0.4 V for TTL devices and 1.06 V for CMOS devices operating at 5 V V_{CC} and driving dc loads.

The guaranteed dc noise margin indicates that a noise excursion of 0.4 V for TTL devices or 1.06 V for CMOS devices is possible without propagating the noise through subsequent logic stages. Although the guaranteed noise margin of TTL devices is 0.4 V, a TTL input typically has a noise margin in excess of 1 V. TTL devices change states as the input voltage passes through a threshhold voltage of about 1.5 V. Since a typical TTL V_{OL} is 0.25 V an input can tolerate 1.25 V of noise before the false signal is propagated. In a system, this noise is comprised of crosstalk components, power plane noise as well as simultaneous switching glitches. [3,4]

The term dc noise margin may seem inappropriate when applied to noise, which in general is an ac factor. For high-speed logic, signals with pulse widths of greater than 30 ns or 40 ns can be considered dc. As pulse durations shorten, a limit is reached where an input pulse can be shorter than the time required for a signal to propagate through the device. As this point is approached, pulses of greater amplitude are required to effect a change at the driven device's output. Eventually any pulse of reasonable amplitude will not be propagated.

End pin ACL devices exhibit simultaneous switching noise pulse widths of 4 ns to 8 ns for pulse amplitudes of 1.7 V to 2.5 V. In order to evaluate the effect of noise with these characteristics, it is necessary to evaluate the ac noise margin of the receiving device. Figure 5 illustrates the ac noise margin 74F logic devices exhibit over a wide range of process and operating condition variances. Figure 5 illustrates a 74F device can erroneously switch for noise glitches with amplitudes of 1.75 V to 2.25 V and pulse duration of 1 ns to 5 ns. The erroneous switching performance of a device due to simultaneous switching induced glitches will be adversely affected by other sources of system noise and levels of dc bias present at its input. These other factors reduce the ac noise margin inherent to the device.

Figure 5. Pulse Duration vs Pulse Amplitude
(Typical 74F Clock Pin Process and Operating Condition Variances)

Simultaneous Switching System Considerations

The first order description of the simultaneous switching noise phenomenon of a simple circuit given in the previous sections is useful to illustrate the primary cause of the glitches. However, there are several environmental factors to be considered which can not be described in simple mathematical terms. In order to evaluate the effects of these factors, experimental results will be presented. Therefore, it also becomes critical to understand the relationship between system applications and characterization data.

The system implementation factors to be evaluated are: lumped capacitive loading at a distance, distributed capacitive loading at a distance, temperature, package options, power supply voltage, lumped ac and dc loading at the device, input signal offsets, input signal edge rates, and circuit propagation delay effects.

Lumped and Distributive Loading (at a distance) Effects

Texas Instruments Advanced High-Speed Logic characterization boards are constructed with lumped ouput loads placed as near the DUT (device under test) as possible. This is necessary to obtain sufficiently clean signals for accurate measurement. Data that has been presented in this paper was obtained using the standard procedure in Appendix A with characterization boards configured as described.

8

Typical system environments do not offer simple lumped loads at the device pins. If transmission lines between receiving devices are short, the environment that the output is driving can appear as lumped capacitive loads some distance away. Longer transmission lines, such as those encountered in bus applications, appear as distributed capacitive loads. In order to evaluate these effects the circuit shown in Figure 6 was constructed. A quad gate device was chosen to drive a 4-inch signal line to a 74HC241 receiver. Test points were defined at 1 inch increments along the signal paths.
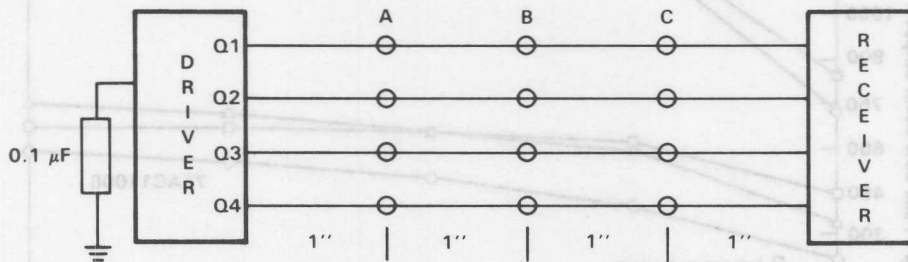

Figure 6. Laboratory Setup for Distributed Loading Evaluation

In testing the effects of lumped capacitive loading away from the device pins, 50 pF loads where placed at test points A or B and V_{OLP} was recorded. As can be seen from Figures 7 and 8, the results of placing the lumped load 1 to 2 inches away from the device under test is a reduction in the magnitude of V_{OLP} at the output of the device under test. However, in a system environment as shown in Figure 6, the magnitude of V_{OLP} at the receiver is approximately the same as that obtained from a characterization board (Figures 9 and 10 can be used for comparison) with the standard loads placed very close to the device under test: for the 74AC00, V_{OLP} is approximately 1.25 V and for the 74AC11008, V_{OLP} is about 0.5 V.

To evaluate the impact of an output driving distributed capacitive loads such as multiple devices on a system bus, 15 pF capacitors were placed at test points A, B, and C (reference Figure 6). V_{OLP} was recorded for both an end pin 74AC00 and Texas Instruments 74AC11008. The results are shown in Figure 11. Once again, the magnitude of the switching noise is reduced at the output of the driving device but at the receiver, the level of V_{OLP} is very near that obtained using an ACL simultaneous switching characterization board.

The major effect of placement of lumped and distributed capacitive loads at a distance away from the driving device is reduction of V_{OLP} or V_{OHV} at the output of the driver. In a system, this is not the point where a switching glitch would be most troublesome. The magnitude of V_{OLP} or V_{OHV} at the input of the receiver

determines whether switching noise will cause a system failure. The values obtained from a system environment correlate very well with the values measured on an ACL simultaneous switching characterization board.

Figure 7. Peak Low-Level Output Voltage vs Distance (Lumped Capacitance at Point A)

10
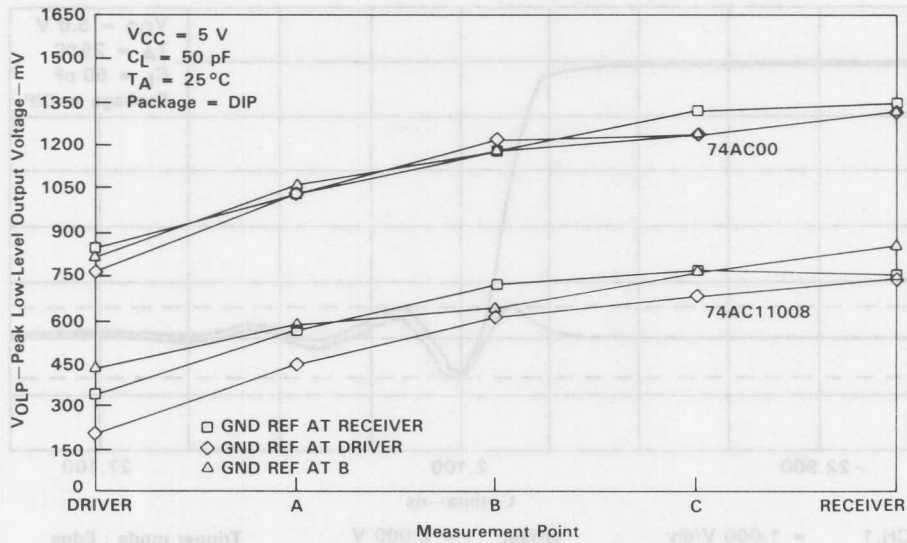
Figure 8. Peak Low-level Output Voltage vs Distance (Lumped Capacitance at Point B)

11

V_{CC} = 5.0 V
T_A = 25°C
C_L = 50 pF
Package = DIP

−22.900   2.100   27.100

t — time — ns
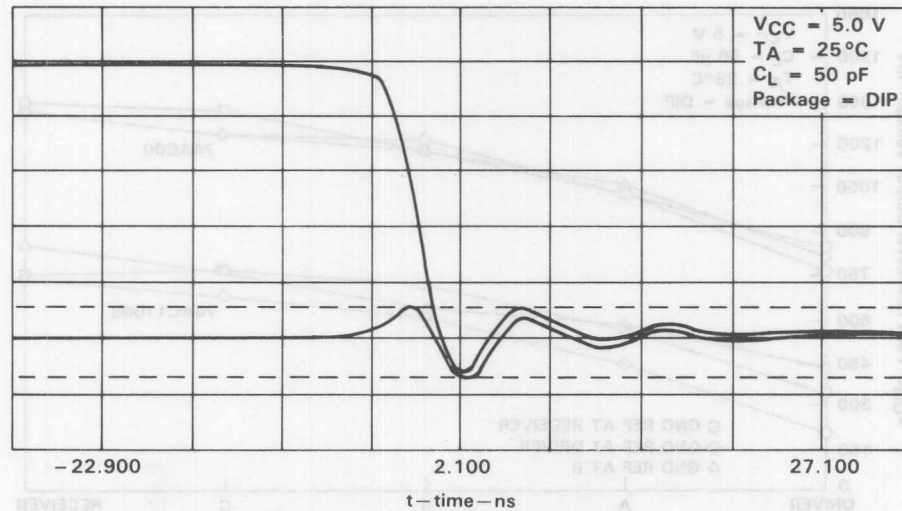
CH.1	= 1.000 V/div	Offset	= 2.000 V	Trigger mode : Edge
CH.2	= 1.000 V/div	Offset	= 2.000 V	On Neg. Edge on Chan2
Timebase	= 5.00 ns/div	Delay	= 2.100 ns	Trigger Levels
Delta V	= 1.240 V			Chan2 = 2.000 V
Vmarker 1 =	−680 mV	Vmarker 2 = 560 mV		Holdoff = 70.000 ns

Figure 9. V_{OLP} Characterization Results for AC11008

12

Vendor # 2
AC00
DC 632
V_{CC} = 5 V
T_A = 25 °C
3/1 switching
V_{IN} = 20% − 80% rail

−34.300   −9.300   15.700

Time−ns

CH.1	= 1.000 V/div		Offset	= 2.000 V
CH.2	= 1.000 V/div		Offset	= 2.000 V
Timebase	= 5.00 ns/div		Delay	= −9.300 ns
Delta V	= 2.320 V			
Vmarker 1	= −940.0 mV		Vmarker 2	= 1.380 V

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 2.000 mV
Holdoff = 70.000 ns
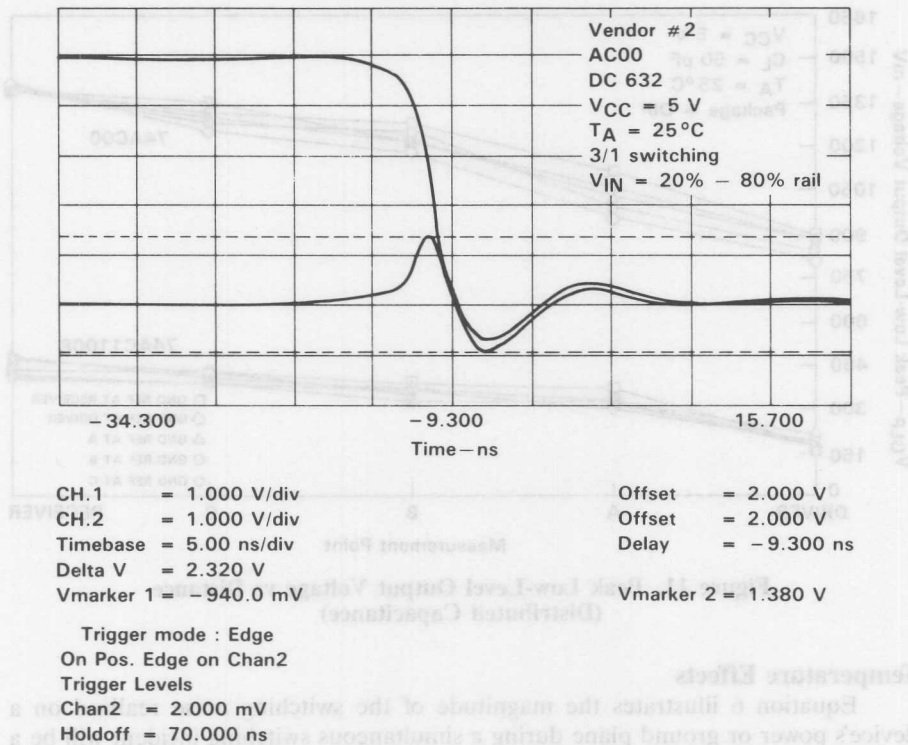
Figure 10. V_{OLP} Characterization Results for AC00

13
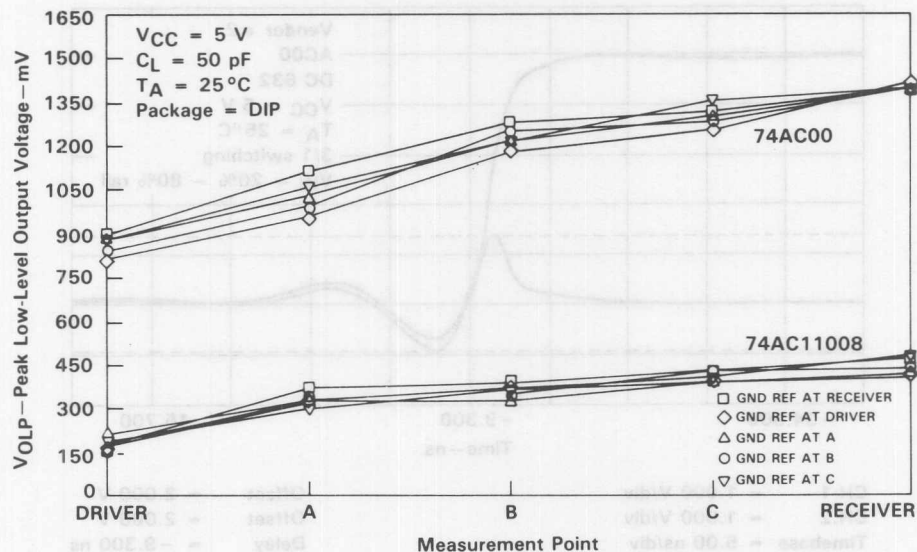
Figure 11. Peak Low-Level Output Voltage vs Distance
(Distributed Capacitance)

Temperature Effects

Equation 6 illustrates the magnitude of the switching noise realized on a device's power or ground plane during a simultaneous switching incident will be a function of the device's output edge rate (dv/dt). As MOS (Metal Oxide Semiconductor) devices operate at lower temperatures they become intrinsically faster. This is due to the inverse temperature dependence of electron and hole mobilities, i.e., as temperature decreases, mobilities increase. [5] Figures 12 through 15 illustrate the effects of temperature upon V_{OLP} and V_{OHV} for other manufactures end pin devices and Texas Instruments ACL devices. Quad gates as well as octal D-type latches are evaluated. Note the increased magnitude of V_{OLP} and the decreased value of V_{OHV} at lower temperatures.

Package Effects

Texas Instruments offers its EPIC™ ACL family functions in surface mount packaging as well as traditional DIP (Dual-in-Line) packaging. Figures 14 and 15 also illustrate the difference in the magnitude of the induced voltage between DIP and SO (Small-Outline) packaged 74AC373 and 74AC11373 devices. A very important observation can be made based upon Figures 14 and 15. The reduction in the magnitude of V_{OLP} and V_{OHV} from DIP to SO packages does not track linearly with the reduction in package inductances as shown in Table 1.

14
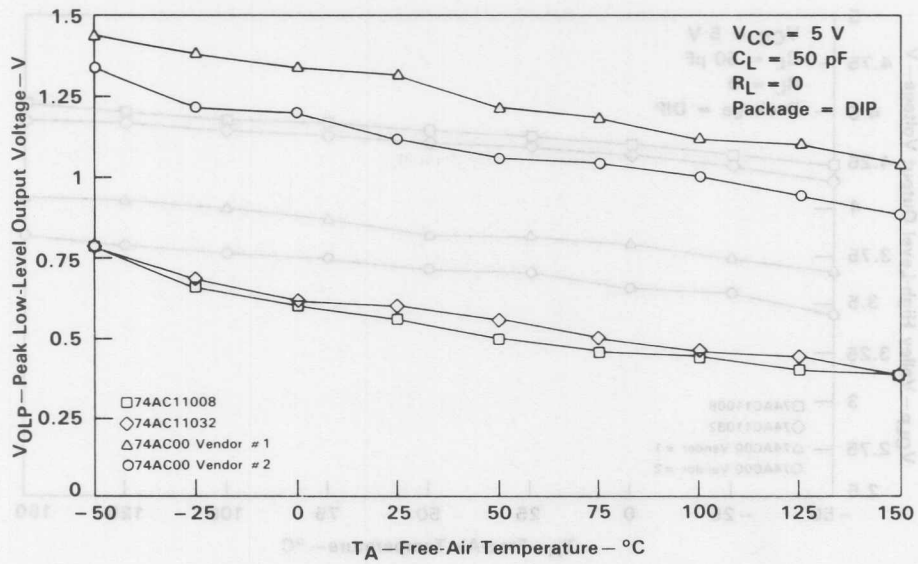
Figure 12. Evaluation of Temperature Effects
Peak Low-Level Output Voltage vs Free-Air Temperature

15

**Figure 13. Evaluation of Temperature Effects
Valley High-Level Output Voltage vs Free-Air Temperature**
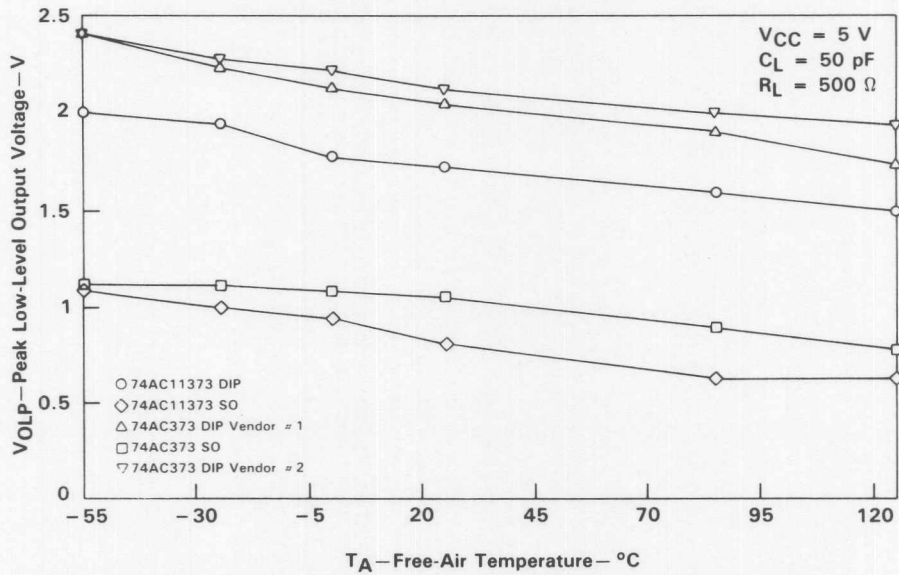
Figure 14. Peak Low-Level Output Voltage vs Free-Air Temperature

16
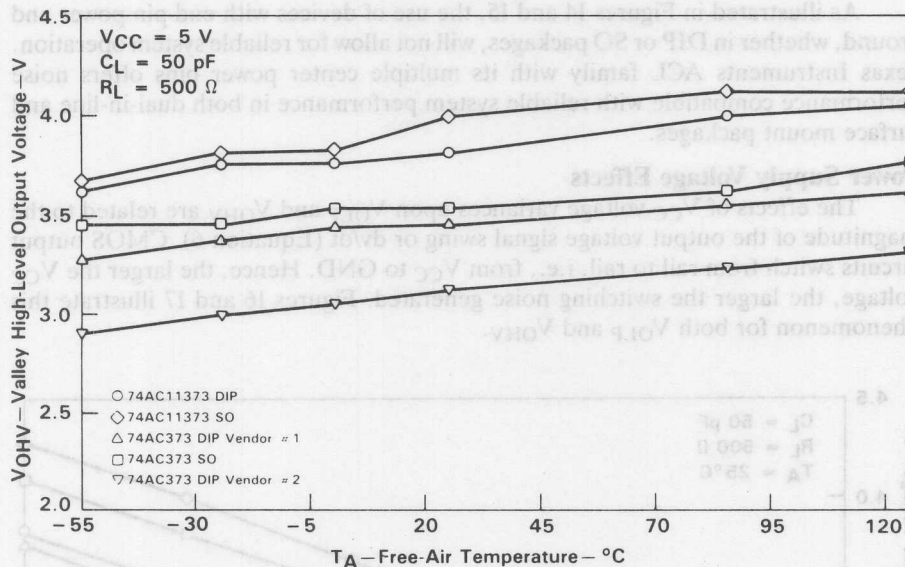
**Figure 15. Valley High-Level Output Voltage vs Free-Air Temperature
(74AC11373 Compared to End-Pin Product)**

**Table 1. Comparison of Dual-in-Line (DIP) and Small Outline (SO) 20-Pin Package
Parasitic Inductances and Percent Change in Switching Noise**

Pin	Dual-in-Line Self-Inductance	Small-Outline Self-Inductance	DIP to SO Percentage Change Self-Inductance	DIP to SO Percentage Change End-Pin V_{OLP}	DIP to SO Percentage Change Center-Pin V_{OLP}
1	13.7 nH	5.8 nH	57%	18%	36%

The reason the magnitude of switching noise is not reduced proportionally to a reduction in package parasitics is the effective positive feedback which exists between the silicon die and the package ground or power pin inductances. A reduction in the package ground or power pin inductance reduces the debiasing effects of the induced noise on the transistors in the circuit. This allows the transistor to switch faster, generating larger dv/dt and more switching noise.

As illustrated in Figures 14 and 15, the use of devices with end pin power and ground, whether in DIP or SO packages, will not allow for reliable system operation. Texas Instruments ACL family with its multiple center power pins offers noise performance compatible with reliable system performance in both dual-in-line and surface mount packages.

Power Supply Voltage Effects

The effects of V_{CC} voltage variances upon V_{OLP} and V_{OHV} are related to the magnitude of the output voltage signal swing or dv/dt (Equation 6). CMOS output circuits switch from rail to rail, i.e., from V_{CC} to GND. Hence, the larger the V_{CC} voltage, the larger the switching noise generated. Figures 16 and 17 illustrate this phenomenon for both V_{OLP} and V_{OHV}.
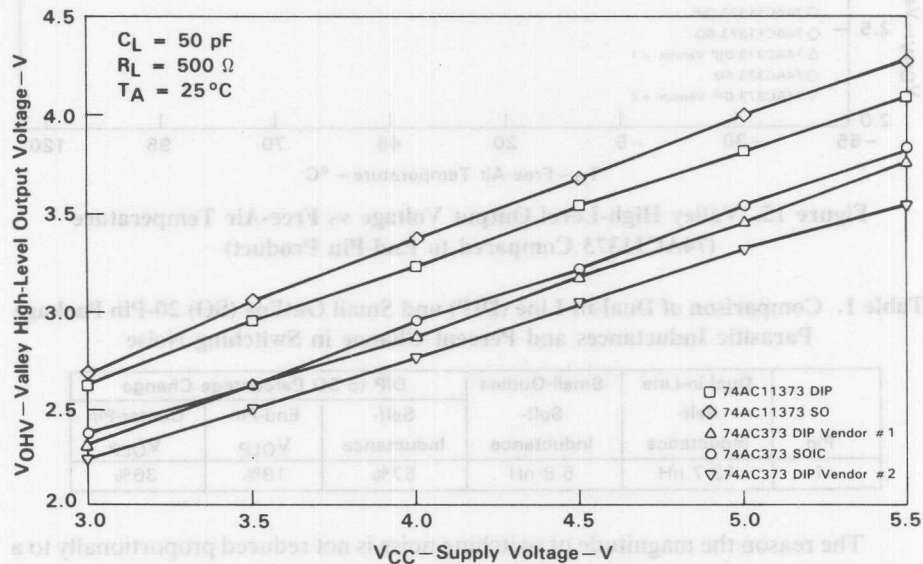
Figure 16. Valley High-Level Output Voltage vs Supply Voltage (74AC11373 Compared to End-Pin Product)

The tradeoff for operation at lower V_{CC} to reduce switching noise is one of speed versus noise. Any advanced CMOS product in the market today has propagation delays specified at $V_{CC} = 5$ V as well as $V_{CC} = 3.3$ V. In general, the propagation delays of an ACL device are 40% slower during 3.3 V operation than at 5 V.

18
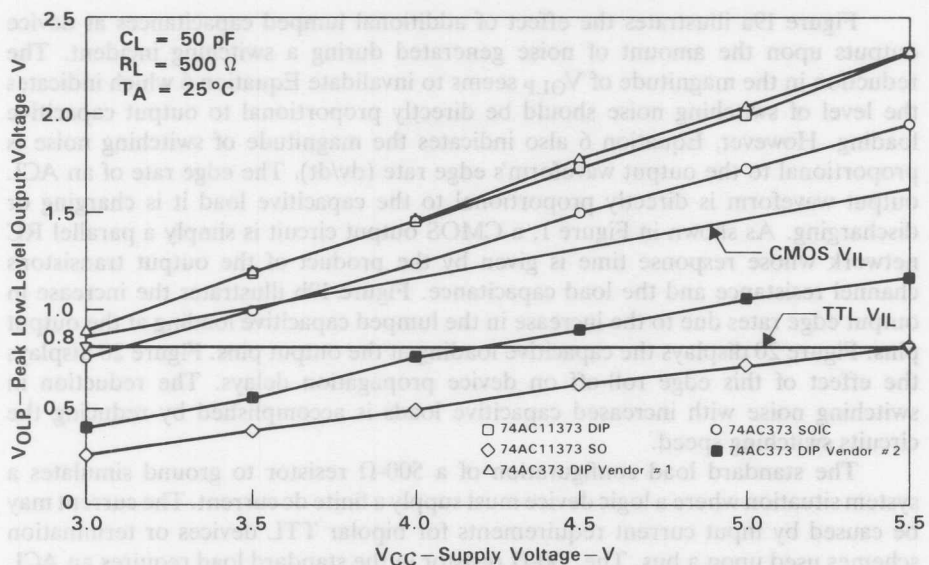
Figure 17. Peak Low-Level Output Voltage vs Supply Voltage (74AC11373 Compared to End-Pin Product)

Lumped AC and DC Loading (at the device) Effects

Advanced high-speed logic devices are characterized, tested and functionally guaranteed with a standard output loading of 50 pF and 500 Ω. Figure 18 illustrates the standard loads for Texas Instruments ACL family. System environments generally offer a variety of capacitive and resistive loads, rather than simple $50-pF/500-\Omega$ loads.
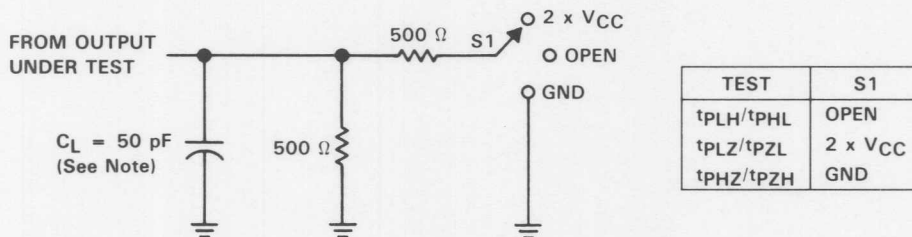
NOTE: C_L includes probe and jig capacitance.

Figure 18. Standard ACL Load Circuit

Figure 19a illustrates the effect of additional lumped capacitances at device outputs upon the amount of noise generated during a switching incident. The reduction in the magnitude of V_{OLP} seems to invalidate Equation 6 which indicates the level of switching noise should be directly proportional to output capacitive loading. However, Equation 6 also indicates the magnitude of switching noise is proportional to the output waveform's edge rate (dv/dt). The edge rate of an ACL output waveform is directly proportional to the capacitive load it is charging or discharging. As shown in Figure 1, a CMOS output circuit is simply a parallel RC network whose response time is given by the product of the output transistor's channel resistance and the load capacitance. Figure 19b illustrates the increase in output edge rates due to the increase in the lumped capacitive loading at the output pins. Figure 20 displays the capacitive loading at the output pins. Figure 20 displays the effect of this edge roll-off on device propagation delays. The reduction in switching noise with increased capacitive loads is accomplished by reducing the circuits switching speed.

The standard load configuration of a 500-Ω resistor to ground simulates a system situation where a logic device must supply a finite dc current. The current may be caused by input current requirements for bipolar TTL devices or termination schemes used upon a bus. The 500-Ω resistor in the standard load requires an ACL device operating at $V_{CC} = 5$ V to provide an output current of approximately 10 mA when the output is in the high state. This current is approximately half of the maximum rated 24-mA output current (I_{OL} or I_{OH}) of an ACL device.

In order to evaluate the effects of other finite dc currents upon V_{OLP} and V_{OHV} simultaneous switching tests were performed over a wide range of I_{OL} and I_{OH} currents. Figures 21 and 22 depict only a slight increase in V_{OHV} and V_{OLP} for dc currents greater than 24-mA. These are expected results because although simultaneous switching is a function of transient current (ac), more charge must be moved during a switching incident when the output is loaded with a dc current.
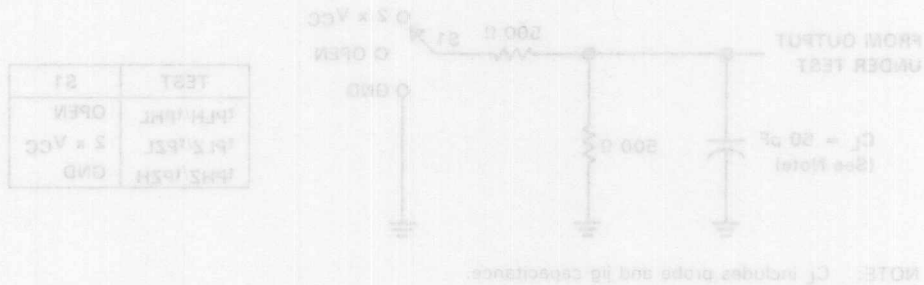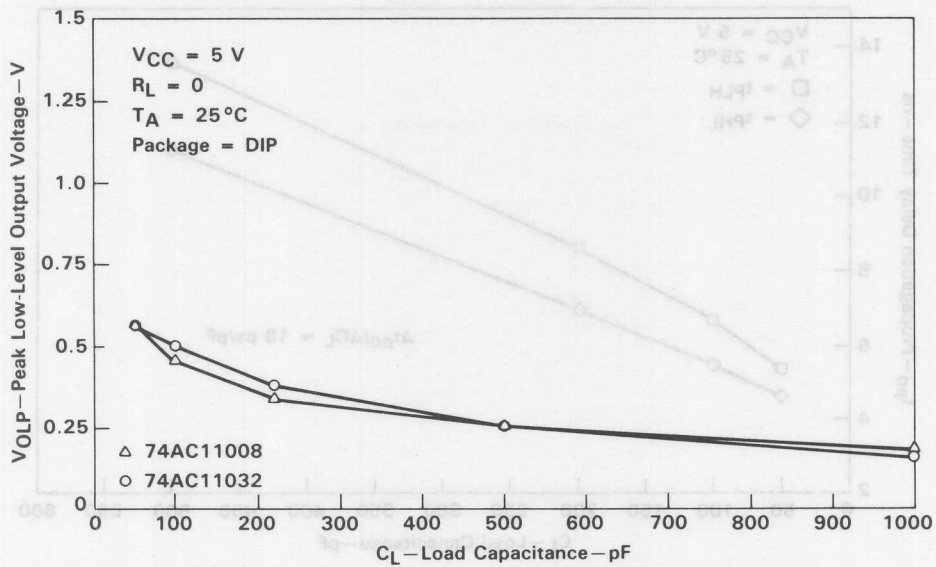
Figure 19a. Loading Effect Evaluation, Peak Low-Level Output Voltage vs Load Capacitance
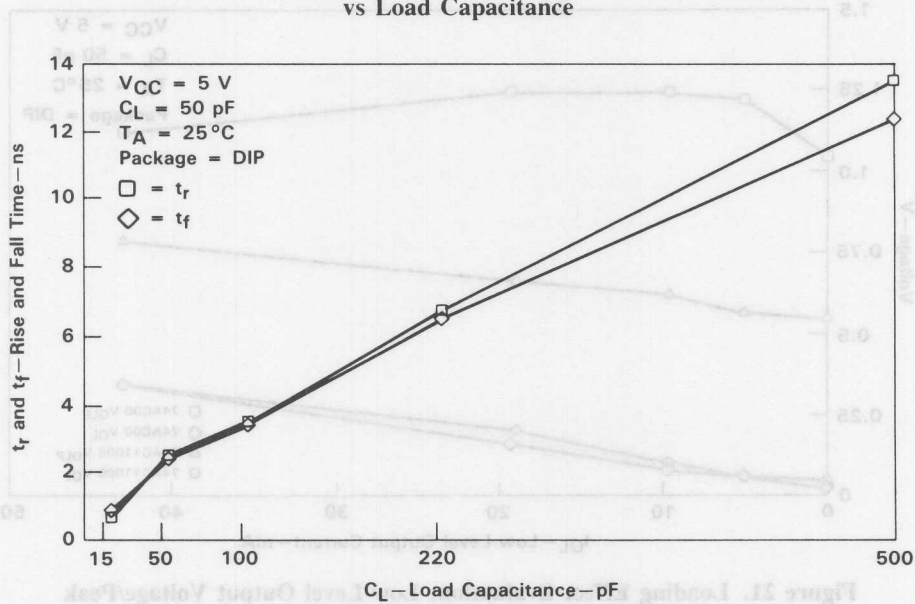
Figure 19b. AC11027 Load Capacitance vs Rise and Fall Times

21
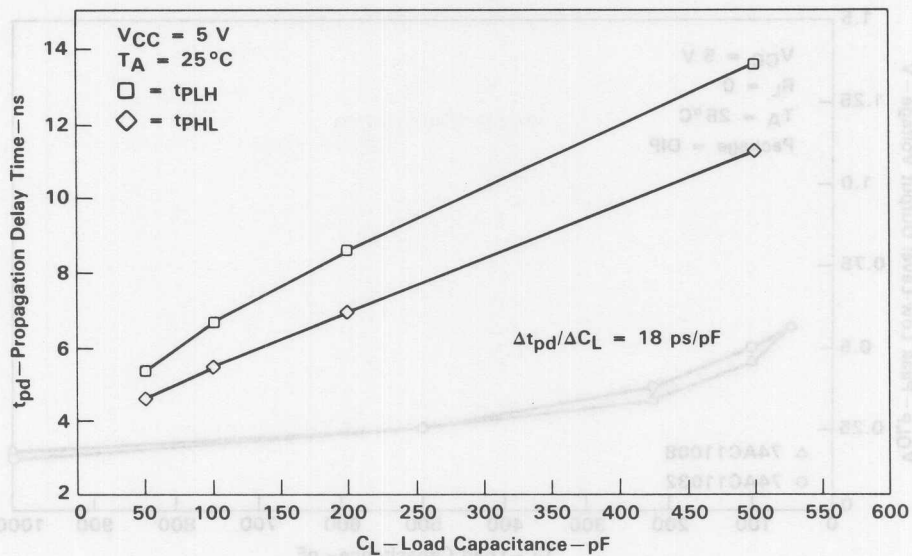
Figure 20. Propagation Delay Time vs Load Capacitance

In Figure 20, the plot shows:
- $V_{CC} = 5$ V
- $T_A = 25\,°C$
- □ = t_{PLH}
- ◇ = t_{PHL}
- $\Delta t_{pd}/\Delta C_L = 18$ ps/pF

Axes: t_{pd}—Propagation Delay Time—ns (vertical), C_L—Load Capacitance—pF (horizontal)
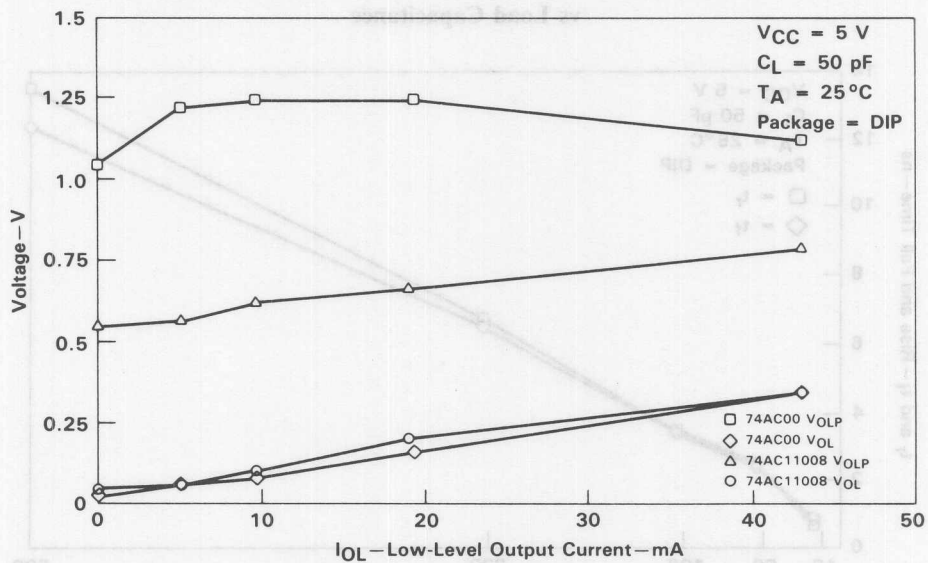
Figure 21. Loading Effect Evaluation, Low-Level Output Voltage/Peak Low-Level Output Voltage vs Low-Level Output Current

In Figure 21, the plot shows:
- $V_{CC} = 5$ V
- $C_L = 50$ pF
- $T_A = 25\,°C$
- Package = DIP
- □ 74AC00 V_{OLP}
- ◇ 74AC00 V_{OL}
- △ 74AC11008 V_{OLP}
- ○ 74AC11008 V_{OL}

Axes: Voltage—V (vertical), I_{OL}—Low-Level Output Current—mA (horizontal)

22
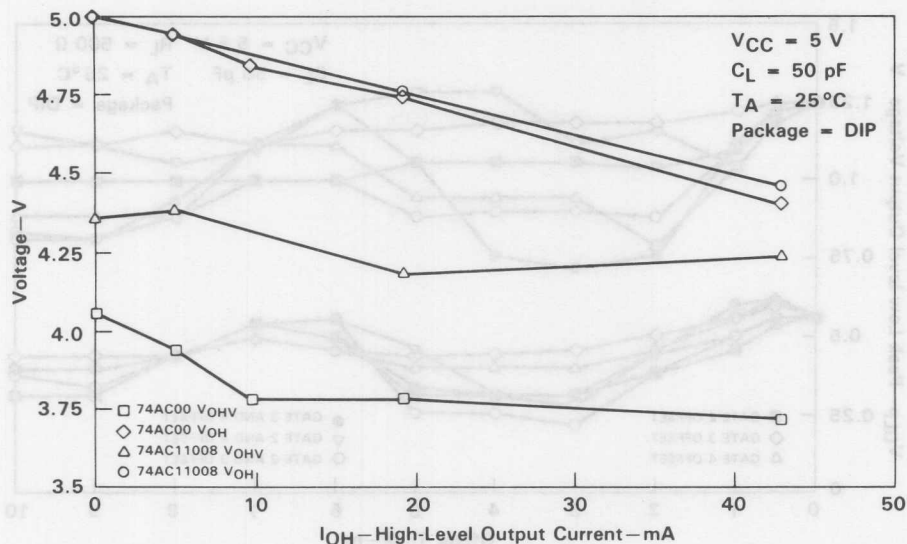
**Figure 22. Loading Effects Evaluation, High-Level Output Voltage/Valley
High-Level Output Voltage vs High-Level Output Current**

Input Signal Offset Effects

In system operation, it can be argued that the occurrence of a perfectly simultaneous switching incident is unlikely to occur due to timing skews in signal paths and semiconductor devices. In order to evaluate a system environment with input signals skewed, an experiment was performed using quad gates. The input signals to each of three gates were supplied using different channels of a high-speed pulse generator while the fourth output on the device was held in a low state. Using the delays of the pulse generator, the input signals were skewed in 1 ns increments for all possible combinations of inputs. V_{OLP} was recorded for each test condition.

Figure 23 illustrates the results for an end pin 74AC00 and Texas Instruments 74AC11032. Note the sinusoid response of V_{OLP} as a function of input signal offset. This effect is caused by the natural frequency of the parasitic tank circuit formed by the load capacitor, channel resistance of the output transistor and the ground pin inductance. For up to 10-ns input signal offsets, the level of V_{OLP} is essentially the same as that of a simultaneous switching incident. This illustrates that even with large values of input signal skew, a device can exhibit large V_{OLP} and V_{OHV} values.

23
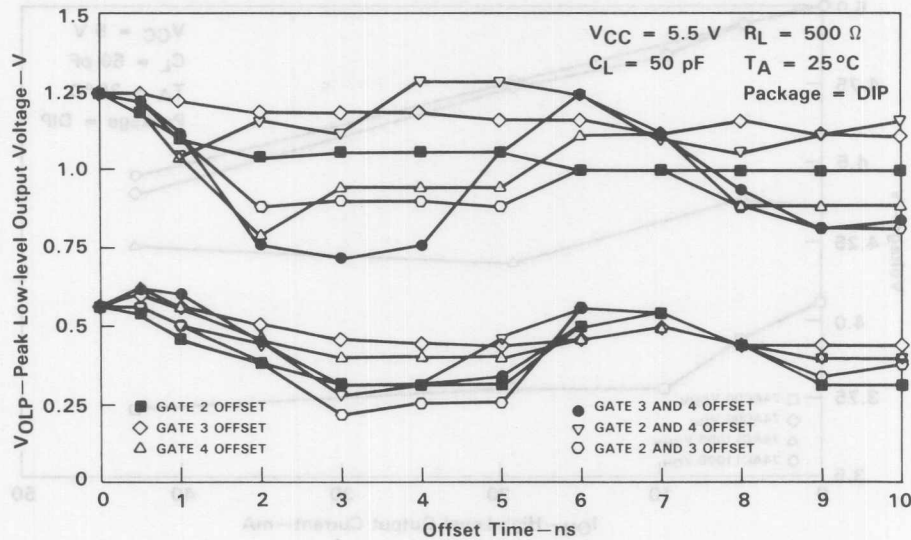
Figure 23. Input Signal Offset Evaluation
(74AC00 vs 74AC11032)

Input Signal Edge Rates

The magnitude of V_{OLP} and V_{OHV} can depend upon the input signal transition time. In order to simulate simultaneous switching phenomenon, several inputs of a device may be tied together. Connecting inputs together can degrade input signal rise and fall times from the specified 3 ns to approximately 8 ns to 10 ns. Studies have been conducted to evaluate the effects of input signal edge rates upon V_{OLP} and V_{OHV}. It has been found that input signal edge rates from 1 ns to 10 ns do not effect the magnitude of V_{OLP} and V_{OHV}. However, it is important for input signals to be properly terminated as near the device as possible so that the input signal edge is monotonic on all input pins.

Propagation Delay Effects

The occurrence of a simultaneous switching incident can affect the propagation delay of an ACL device. As explained in a previous section, the amplitude of the voltage induced on the silicon die increases as the number of outputs switching simultaneously increases. This induced voltage artificially increases or decreases the threshold of the device. As the switching threshold varies, the time required for the signal to propagate from the input to the output varies accordingly, depending on the input transition and the phase of the ground bounce with respect to the transition.

24

Texas Instrument tests propagation delay effects due to simultaneously switching outputs in the design characterization process. This test is not a production test, but is performed only on the bench during characterization. The test is performed at the nominal conditions of $V_{CC} = 5$ V and $T_A = 25°C$ with standard data book loads and waveforms. A comparison is made of the propagation delay with 1, N/2 and N outputs switching simultaneously. The input transition edge is 3 ns. Propagation delay data for an AC11373 is included in Table 2. This data indicates that both t_{PLH} and t_{PHL} increase with the number of outputs switching. Table 3 includes data for an AC11244 switching in and out of a 3-state condition. The trend in this situation is for the propagation delay to decrease when switching into 3-state as the number of outputs switching increases, and to increase when switching out of 3-state.

Table 2. Propagation Delay Effects Due to Simultaneous Switching on an AC11373, Output IQ.

	NUMBER OF OUTPUTS SWITCHING		
	1	4	8
t_{PLH}	6.69	7.65	8.88
t_{PHL}	6.27	6.70	7.51

Table 3. Propagation Delay Effects Due to Simultaneous Switching on an AC11244, Output 1Y1.

	NUMBER OF OUTPUTS SWITCHING		
	1	4	8
t_{PZH}	6.43	6.91	7.60
t_{PHZ}	6.03	5.82	5.70

The trends indicated from this data are common. However, the trends may vary from device to device as well as from test fixture to test fixture. Skews in input edge signals and variance in input edge rates can affect the trends.

Simultaneous Switching Evaluation

The many factors influencing device simultaneous switching performance require careful consideration before a standard test methodology can be implemented. These factors can be grouped into test board considerations, measurement considerations, and characterization environment considerations. Test board considerations include the physical make-up of the board and signal loading. Pin location, ground reference, and scope equipment are included in measurement considerations. Characterization environment considerations include power supply voltage, ambient temperature, and input signal characteristics. A standard simultaneous switching test methodology for the EPIC™ ACL family is presented in Appendix A.

Test Board Considerations

The simultaneous switching test board is a multilayer 50-Ω board displayed in Figures 24 and 25. A parts list with vendor information is provided in Appendix B. Multiple ground and V_{CC} planes minimize power node inductance and are commonly found in high-speed system boards. Signal traces run equal lengths to barrel connectors which offer a reduced inductance seat for the device under test. Though barrel connectors are not usually used in systems, data from another

6.500

7.500
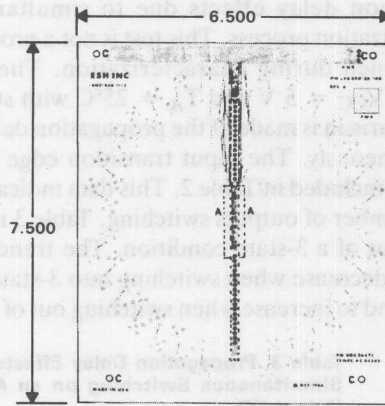
TOP METAL
(VIEWED FROM TOP)
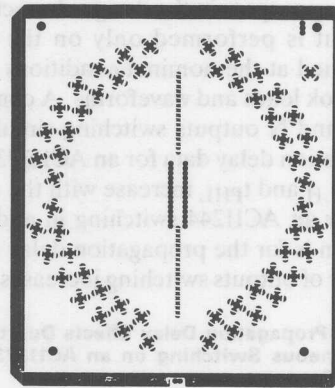
LAYER 2
VIEWED FROM TOP
METAL IS CLEAR
GND
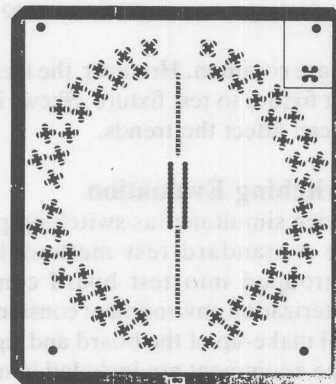
LAYER 3
VIEWED FROM TOP
METAL IS CLEAR
GND
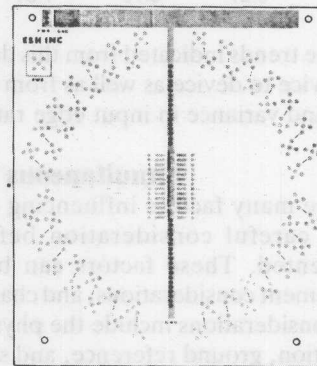
BOTTOM METAL
(VIEWED FROM BOTTOM)

LAYER 1	CU	0.0014
	DIELECTRIC	0.010 ± 0.0015
2	CU	0.0014
	ADJUST FOR THICKNESS	
3	CU	0.0014
	DIELECTRIC	0.010 ± 0.0015
4	CU	0.0014

Figure 24. Board Layout and Composition

26
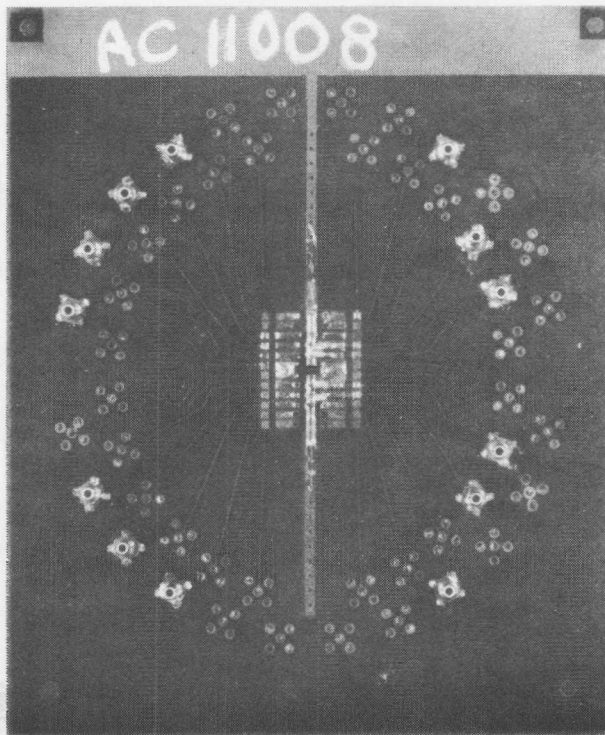
Figure 25. Board Photograph

manufacturer's AC240 in Figure 26a shows that they yield the same results as a soldered device in Figure 26b. Since logic gate switching can cause large current transients, a decoupling capacitor of 0.1 μF is used between the power rails.

Due to the high-speed signals that will be used to test the device, ac loading becomes a critical part of the setup. The device under test must not operate in an environment of mismatched transmission lines. Therefore, in addition to the use of proper values for ac loading, the placement of the loads on the board is critical. For example, input signal traces are terminated in 50-Ω resistors at the device input pins, instead of at the Sealectro RF connector, for proper termination of the 50-Ω coax cables used to connect the SPG (Signal Pulse Generator) to the board. The termination at the device pins is easily accommodated through the use of the center ground strip on the simultaneous switching board (reference Figures 24 or 25). Output signal traces are terminated with a 47-pF capacitor at the pin with a 450-Ω

27

$V_{OHV} = 3.44$ V

$V_{CC} = 5$ V
$C_L = 50$ pF
$T_A = 25°C$
PACKAGE = DIP

9.600   34.600   59.600

Time – ns

CH.1 = 1.000 V/div	Trigger mode : Edge	Offset = 3.000 V
CH.2 = 1.000 V/div	On Pos. Edge on Trig3	Offset = 3.000 V
Timebase = 5.00 ns/div	Trigger Levels	Delay = 34.600 ns
Delta V = 2.500 V	Trig 3 = 750.00 mV	
Vmarker 1 = 3.440 V	Holdoff = 70.000 ns	Vmarker 2 = 5.940 V

Vendor #2
AC240
7/1 switching
$V_{IN} = 20\% - 80\%$

$V_{OLP} = 2.1$ V

$V_{CC} = 5$ V
$C_L = 50$ pF
$T_A = 25°C$
PACKAGE = DIP

9.700   34.700   59.700

Time – ns
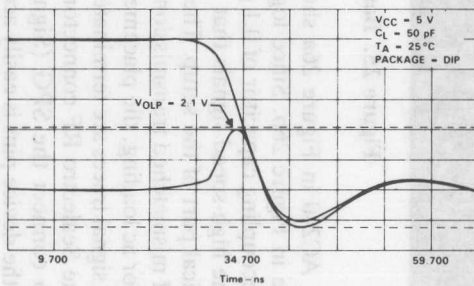
CH.1 = 1.000 V/div	Trigger mode : Edge	Offset = 2.000 V
CH.2 = 1.000 V/div	On Pos. Edge on Trig3	Offset = 2.000 V
Timebase = 5.00 ns/div	Trigger Levels	Delay = 34.700 ns
Delta V = 3.320 V	Trig 3 = 750.00 mV	
Vmarker 1 = 1.260 V	Holdoff = 70.000 ns	Vmarker 2 = 2.060 V

**Figure 26a. Data Taken with
Device in Barrel Connectors**

$V_{OHV} = 3.44$ V

$V_{CC} = 5$ V
$C_L = 50$ pF
$T_A = 25°C$
PACKAGE = DIP

11.500   36.500   61.500

Time – ns

CH.1 = 1.000 V/div	Trigger mode : Edge	Offset = 2.000 V
CH.2 = 1.000 V/div	On Pos. Edge on Trig3	Offset = 2.000 V
Timebase = 5.00 ns/div	Trigger Levels	Delay = 36.500 ns
Delta V = 2.460 V	Trig 3 = 750.00 mV	
Vmarker 1 = 3.440 V	Holdoff = 70.000 ns	Vmarker 2 = 5.900 V

Vendor #2
AC240
7/1 switching
$V_{IN} = 20\% - 80\%$

$V_{OLP} = 2.1$ V

$V_{CC} = 5$ V
$C_L = 50$ pF
$T_A = 25°C$
PACKAGE = DIP

11.800   36.800   61.800

Time – ns
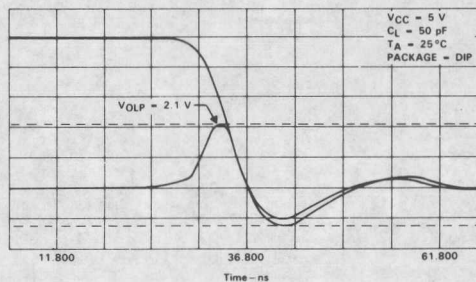
CH.1 = 1.000 V/div	Trigger mode : Edge	Offset = 2.000 V
CH.2 = 1.000 V/div	On Pos. Edge on Trig3	Offset = 2.000 V
Timebase = 5.00 ns/div	Trigger Levels	Delay = 36.800 ns
Delta V = 3.360 V	Trig 3 = 750.00 mV	
Vmarker 1 = –1.260 V	Holdoff = 70.000 ns	Vmarker 2 = 2.100 V

**Figure 26b. Data Taken with
Device Soldered to Board**

resistor in series with the trace. Correct ACL dc output resistive loading is achieved through either a 50-Ω terminator or a 50-Ω scope probe at the Sealectro RF connector.

Measurement Considerations

The device pin with the largest total inductance (i.e., self plus mutual) produces worst-case results and should be used as the test pin. The inductive noise versus pin location is displayed in Figure 27. As expected, the pins farthest from the center of the package have larger values of inductive noise. However, the worst-case noise may not be observed on the corner pins, rather it could occur on their adjacent neighbors. This is not surprising since corner pins can have a lower value of mutual coupling to active pins than their neighbors. This effect is negated by a much larger
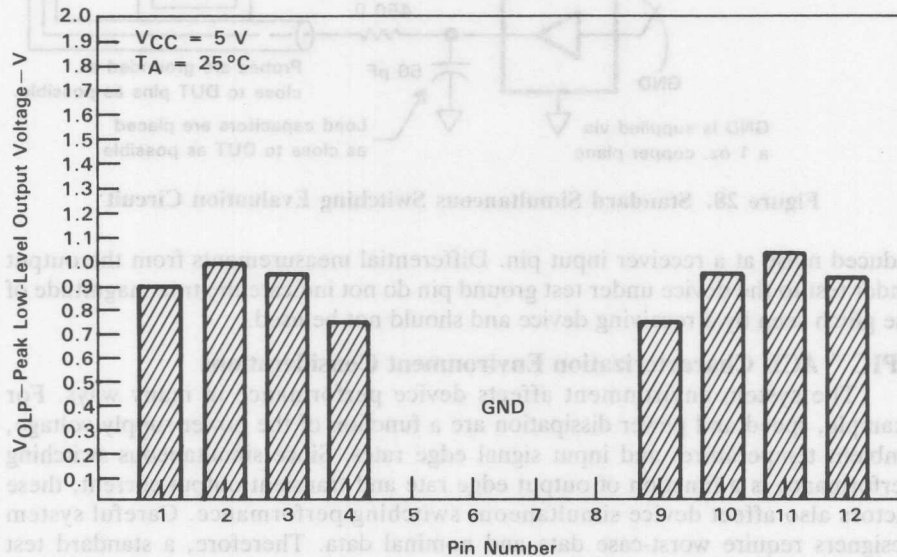
Figure 27. AC11240 Peak Low-Level Output Voltage vs Pin Location

drop in the self inductances as the pin locations get closer to the center of the package. Since different package types will exhibit slightly different characteristics, worst-case pin locations will vary with package and device type.

The correct setup for accurate measurement of simultaneous switching events is displayed in Figure 28. The scope is an HP5411OD with a 1 Ghz bandwidth. Scopes with smaller bandwidths are not recommended due to the high frequency components of the inductive voltages that will be translated as data by high speed logic devices. Probes are standard 50-Ω coax that attach to Sealectro RF connectors

on the test board. These probes complete the 500-Ω resistive loading on the device output pins and their ground reference is the ground plane of the simultaneous switching board. This setup allows absolute measurement of the magnitude of the
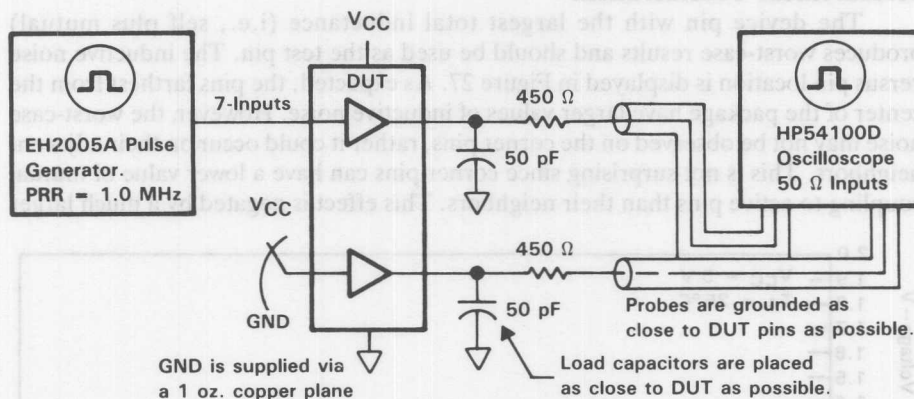
Figure 28. Standard Simultaneous Switching Evaluation Circuit

induced noise at a receiver input pin. Differential measurements from the output under test to the device under test ground pin do not indicate the true magnitude of the glitch seen by a receiving device and should not be used.

EPIC™ ACL Characterization Environment Considerations

The system environment affects device performance in many ways. For example, speed and power dissipation are a function of the power supply voltage, ambient temperature, and input signal edge rates. Since simultaneous switching performance is a function of output edge rate and transient output current, these factors also affect device simultaneous switching performance. Careful system designers require worst-case data and nominal data. Therefore, a standard test methodology includes both data points. Texas Instruments characterizes EPIC™ ACL devices at nominal conditions of $V_{CC} = 5$ V and $T_A = 25°C$ and worst-case conditions of $V_{CC} = 5.5$ V and $T_A = -55°C$ since the family is offered with military specifications. Commercial users should expect improved worst-case performance at the minimum specified temperature of $-40°C$. The procedure in Appendix A is offered as a standard evaluation of simultaneous switching performance. It has been adapted specifically to the EPIC™ ACL family of devices, but testing other families requires only minor modifications of data sheet parameters such as maximum V_{CC}, input voltage swings, etc.

Sample nominal data from each of the three simultaneous switching tests are displayed in Figures 29, 30, and 31. Correct data can only be obtained through careful use of a standard test methodology. The physical make-up of the test board, signal termination, test pin location, ground reference, and scope equipment are factors that must be considered. It is also important to recognize the system environment and consider power supply voltage, ambient temperature, and input signal characteristics. The standard test methodology must be applicable to all families, bipolar or CMOS. Although the above procedure has been tailored to the EPIC™ ACL family of devices, minor modifications of V_{IH}, V_{IL}, and V_{CC} will allow application of this procedure to other families.
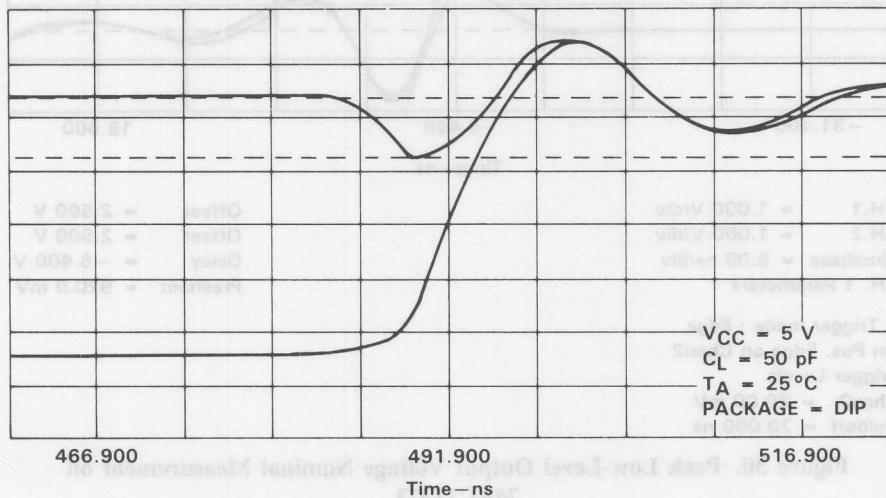
V_{CC} = 5 V
C_L = 50 pF
T_A = 25 °C
PACKAGE = DIP

Time — ns

CH.1	= 1.000 V/div	
CH.2	= 1.000 V/div	
Timebase	= 5.00 ns/div	
Delta V	= 1.120 V	
Vmarker 1	= 3.740 V	

Offset = 2.500 V
Offset = 2.500 V
Delay = 491.900 ns

Vmarker 2 = 4.860 V

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 20.00 mV
Holdoff = 70.000 ns

Figure 29. V_{OHV} Nominal Measurement on 74AC11373

```
                                              VCC = 5 V
                                              CL = 50 pF
                                              TA = 25°C
                                              PACKAGE = DIP
```

- 31.400   - 6.400   18.600

Time—ns

CH.1   = 1.000 V/div   Offset   = 2.500 V
CH.2   = 1.000 V/div   Offset   = 2.500 V
Timebase = 5.00 ns/div   Delay   = - 6.400 V
CH. 1 Parameters   Preshoot = 920.0 mV

 Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2   = 20.00 mV
Holdoff = 70.000 ns
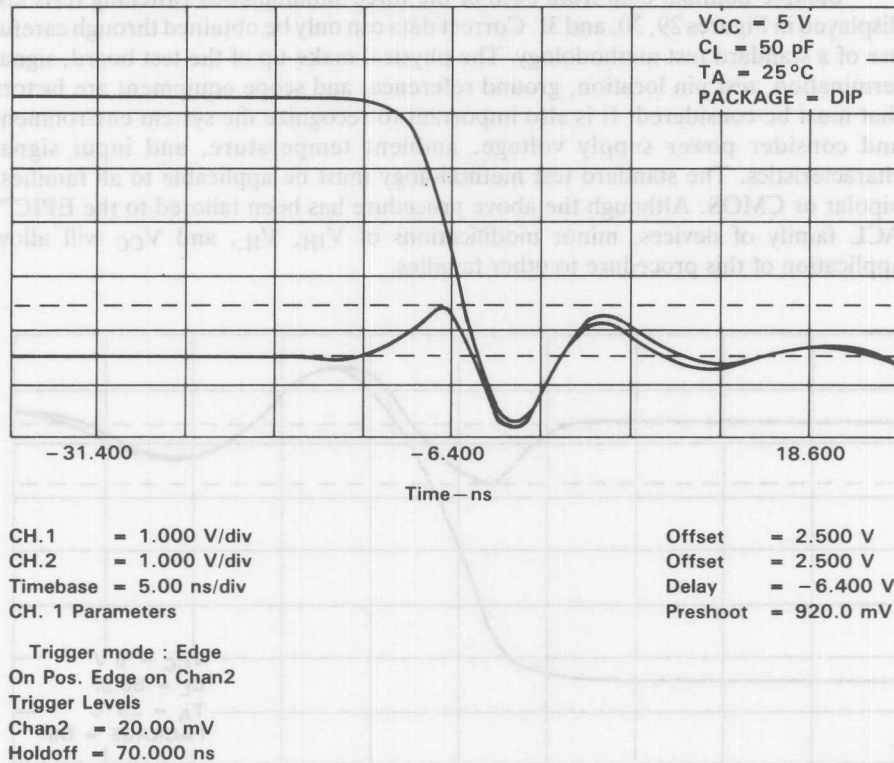
**Figure 30. Peak Low-Level Output Voltage Nominal Measurement on
74AC11373**
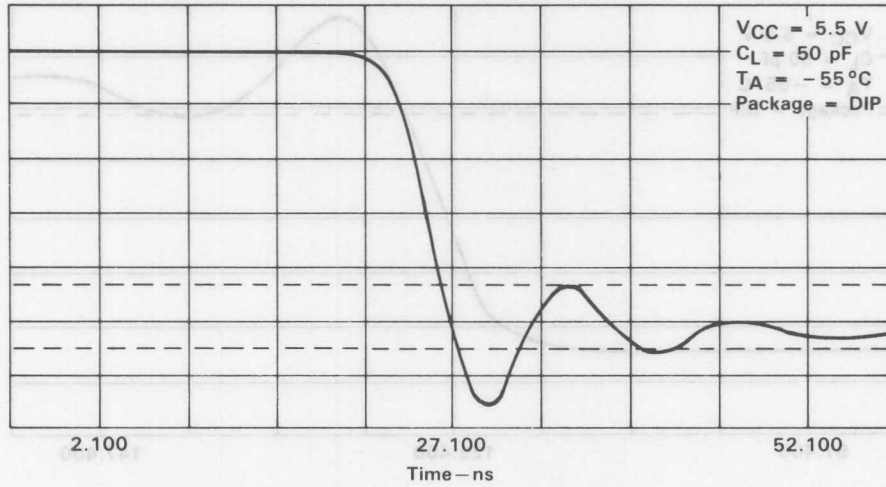
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 1.200 V
Vmarker 1 = 0.000 V

Offset = 2.500 V
Delay = 27.100 ns

Vmarker 2 = 1.200 V

Trigger mode : Edge
On Pos. Edge on Trig3
Trigger Levels
Trig3 = 250.0 mV
Holdoff = 70.000 ns

**Figure 31a. 74AC11373 Passes Stored Data Test on the
High Impedance to Low Transition (ZL)**

Figure 31b. 74AC11373 Passes Stored Data Test on the
High Impedance to High Transition (ZH)

V_{CC} = 5.5 V
C_L = 50 pF
T_A = −55 °C
Package = DIP

97.400   122.400   147.400

CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 1.100 V
Vmarker 1 = 4.400 V

Trigger mode : Edge
On Pos. Edge on Trig3
Trigger Levels
Trig3 = 2.000 V
Holdoff = 70.000 ns

Offset = 2.500 V
Delay = 122.400 ns

Vmarker 2 = 5.500 V
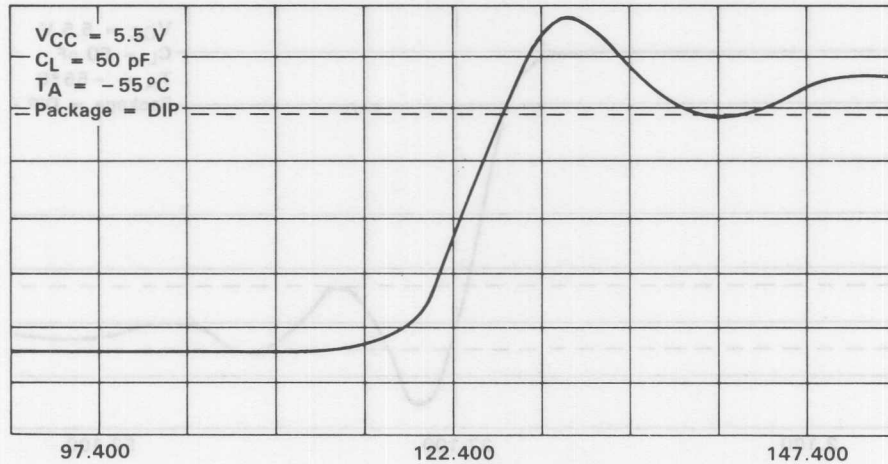
Conclusion

This application report has presented a description of the simultaneous switching issues applicable to high-speed logic devices and systems. The phenomenon was described with a simple first-order model to demonstrate the effect package parasitics and device physics have upon V_{OLP} and V_{OHV}. In order to give the designer a feel for system effects on V_{OLP} and V_{OHV}, several factors have been presented. These factors include: power supply variances, temperature effects, package and pinout issues, ac and dc loading effects, distributed and lumped capacitive loading at a distance, input signal skews, and input signal edge rates.

The purpose of the descriptions and data presented in this report is to allow the system design engineer to recognize the impact simultaneous switching noise may have upon a system. However, it is not realistic for Texas Instruments to totally characterize devices for every possible system environment. The final responsibility for implementing high-speed logic devices lies with the system designer. Texas Instruments has attempted to make this task as simple as possible by using innovative packaging techniques and circuit design techniques in the EPIC™ ACL family.

A standard test methodology has also been presented. This methodology has been developed in conjunction with Phillips/Signetics (Texas Instruments co-developers of the EPIC™ ACL family.) This test method has been shown to correlate with the level of switching noise developed by a circuit in a system environment.

References

1. "Computing Inductive Noise of Chip Packages," A.J. Rainal, *AT&T Bell Laboratories Technical Journal Vol. 63*, No. 1, January 1984.
2. "Designing with TTL Integrated Circuits," *Texas Instruments Electronic Series*, Edited by Robert L. Morris and John R. Miller.
3. "AS Load Management," Michael A. Higgs, Texas Instruments, Application Report, 1987.
4. "One Micron Advanced Logic," Chas. Hefner, et al., *Wescon/86* Session 22, November 18-20, 1986.
5. "MOS/LSI Design and Application," *Texas Instruments Electronic Series*, Edited by William N. Carr and Jack P. Mize.

Acknowledgment

Conclusion

This application report has presented a description of the simultaneous switching issues applicable to high-speed logic devices and systems. The phenomenon was described with a simple first-order model to demonstrate the effect package parasitics and device physics have upon V_{OLP} and V_{OHV}. In order to give the designer a feel for system effects on V_{OLP} and V_{OHV}, several factors have been presented. These factors include: power supply variances, temperature effects, package and pinout issues, ac and dc loading effects, distributed and lumped capacitive loading at a distance, input signal skews, and input signal edge rates.

The purpose of the descriptions and data presented in this report is to allow the system design engineer to recognize the impact simultaneous switching noise may have upon a system. However, it is not realistic for Texas Instruments to totally characterize devices for every possible system environment. The final responsibility for implementing high-speed logic devices lies with the system designer. Texas Instruments has attempted to make this task as simple as possible by using innovative packaging techniques and circuit design techniques in the EPIC™ ACL family.

A standard test methodology has also been presented. This methodology has been developed in conjunction with Phillips/Signetics (Texas Instruments co-developers of the EPIC™ ACL family.) This test method has been shown to correlate with the level of switching noise developed by a circuit in a system environment.

References

1. "Computing Inductive Noise of Chip Packages," A. J. Rainal, AT&T Bell Laboratories Technical Journal Vol. 63, No. 1, January 1984.
2. "Designing with TTL Integrated Circuits," Texas Instruments Electronic Series, Edited by Robert L. Morris and John R. Miller.
3. "AS Load Management," Michael A. Biggs, Texas Instruments, Application Report, 1987.
4. "One Micron Advanced Logic," Chas. Hefner et al., Wescon/86 Session 22, November 18-20, 1986.
5. "MOS/LSI Design and Application," Texas Instruments Electronic Series, Edited by William N. Carr and Jack P. Mize.

Acknowledgment

Appendix A

Simultaneous Switching Test Procedure

The simultaneous switching test as defined in Section 1 will be used to determine the magnitude of output disturbances during simultaneous switching of other outputs. In all cases except for devices with single outputs or single complementary outputs, the output under test is not switching. Section 2 gives the procedure of evaluating this class of devices.

A procedure is also given for evaluating stored data integrity. Specifically, the stored data test consists of monitoring the output of one gate with a stored data bit while the other outputs are simultaneously switching. If the induced noise on the clock or latch enable pin is sufficient to clock or latch new data, then a failure is recorded. Sample stored data integrity test data is shown in Figure A-5. The input edge rate on all simultaneous switching tests is 3 ns.

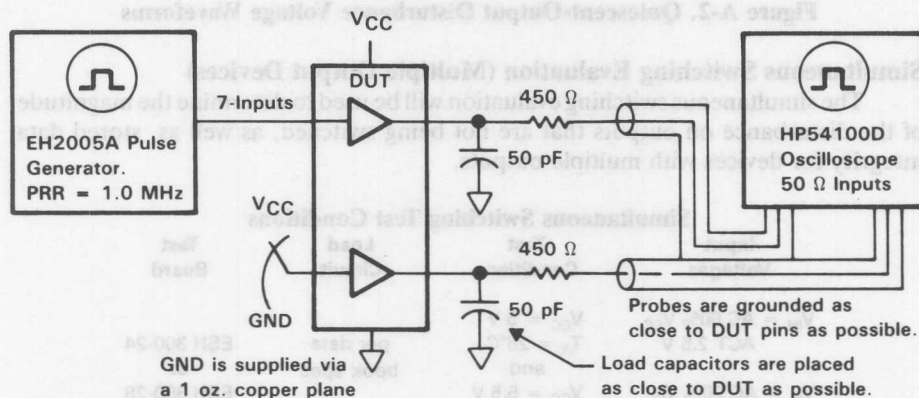**Figure A-1. Standard Simultaneous Switching Evaluation Circuit**

The terms V_{OHV} and V_{OLP} will be used to describe the output disturbance during simultaneous switching as shown in Figures A-2 through A-4. V_{OHV} is defined as the minimum (valley) high-level output voltage during switching. V_{OLP} is defined as the maximum (peak) low-level output voltage during switching of other outputs.
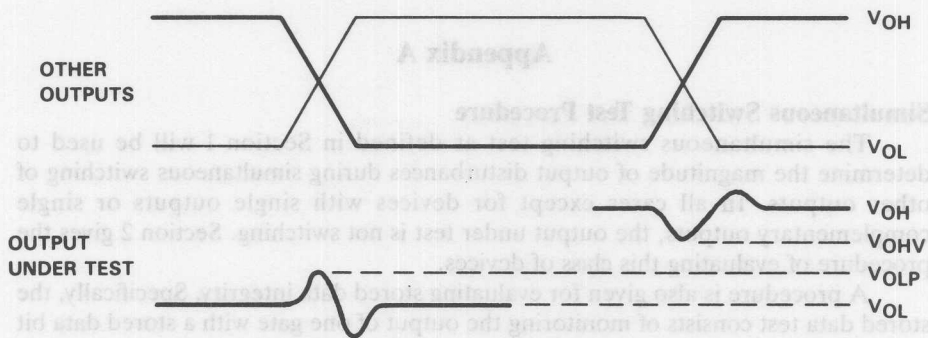
OTHER OUTPUTS — V_{OH}, V_{OL}

OUTPUT UNDER TEST — V_{OH}, V_{OHV}, V_{OLP}, V_{OL}

NOTES: A. V_{OHV} and V_{OLP} are measured with respect to ground reference near the output under test.
B. Input pulses have the following characteristics: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 1 ns.

Figure A-2. Quiescent-Output Disturbance Voltage Waveforms

Simultaneous Switching Evaluation (Multiple Output Devices)

The simultaneous switching evaluation will be used to determine the magnitude of the disturbance on outputs that are not being switched, as well as, stored data integrity for devices with multiple outputs.

Simultaneous Switching Test Conditions

Input Voltages	Test Conditions	Load Circuit	Test Board
V_{IH} = AC 80% V_{CC} ACT 2.5 V	V_{CC} = 5 V T_A = 25°C and	per data book spec	ESH 300-24 or
V_{IL} = AC 20% V_{CC} ACT 0.5 V	V_{CC} = 5.5 V T_A = 55°C		ESH 300-28

V_{OHV} and V_{OLP} are measured with respect to a ground reference near the output under test. Input pulses have the following characteristics: pulse repetition rate 1 MHz, tr = 3 ns, tf = 3 ns, and skew ≤ 1 ns.

Output High Disturbance Test

1. The output to be evaluated will be the output whose pin exhibits the largest magnitude of V_{OHV}.

2. Set input conditions so that the output under test is at a high-logic level.

3. Switch the remaining outputs and observe/record the unswitched output induced voltage, V_{OHV}. See Figure A-3.

4. The outputs should be evaluated for standard t_{PLH} and t_{HPL} transistions as well as by taking the devices in and out of 3-state, if applicable.

V_{OHV}

V_{CC}	= 5 V
C_L	= 50 pF
T_A	= 25 °C
PACKAGE	= DIP

466.900   491.900   516.900

Time — ns

CH.1 = 1.000 V/div
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 1.120 V
Vmarker 1 = 3.740 V

Offset = 2.500 V
Offset = 2.500 V
Delay = 491.900 ns

Vmarker 2 = 4.860 V

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 20.00 mV
Holdoff = 70.000 ns

Figure A-3. V_{OHV} Nominal Measurement on 74AC11373

Output Low Disturbance Test

1. The output to be evaluated will be the output whose pin exhibits the largest magnitude of induced voltage.

2. Set input conditions so that the output under test is at a low-logic level.

3. Switch the remaining outputs and observe/record the unswitched output induced voltage, V_{OLP}. See Figure A-4.

4. The outputs should be evaluated for standard t_{PLH} and t_{PHL} transistions as well as by taking the devices in and out of 3-state, if applicable.

Figure A-4. V_{OLP} Nominal Measurement on 74AC11373

$V_{CC} = 5$ V
$C_L = 50$ pF
$T_A = 25\,°C$
Package = DIP

-31.400 -6.400 18.600

Time—ns

CH.1   = 1.000 V/div
CH.2   = 1.000 V/div
Timebase = 5.00 ns/div
CH. 1 Parameters

    Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2   = 20.00 mV
Holdoff = 70.000 ns
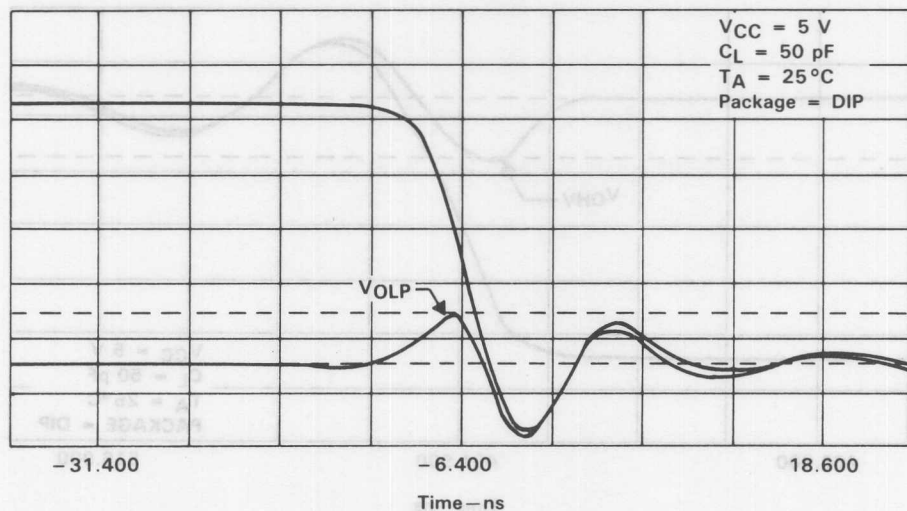
Offset   = 2.500 V
Offset   = 2.500 V
Delay   = −6.400 ns
Vmarker 2 = 920.0 V

Stored Data Integrity

1. Devices with internal storage elements will also have this test performed in addition to the other output glitch evaluation tests. This test will be performed only with worst-case conditions of $V_{CC} = 5.5$ V, $T_A = -55\,°C$.

2. Store a known bit of data in an internal storage element. The element should be the element with the same output as the one used for V_{OHV} and V_{OLP} tests.

3. Switch all remaining outputs or all outputs if possible and check to see that data is not destroyed. The method of switching the outputs can vary from device to device. In the case of devices with 3-state outputs, the worst-case test will be to disable the output, pull the output to the opposite logic state of the enabled output, then enable the output. See Figure A-5.

4. Storage of both high and low level data will be evaluated.

V$_{CC}$ = 5.5 V		
C$_L$ = 50 pF		
T$_A$ = −55°C		
Package = DIP		

2.100   27.100   52.100

Time—ns

CH.2   = 1.000 V/div   Offset   = 2.500 V
Timebase = 5.00 ns/div   Delay   = 27.100 ns
Delta V   = 1.200 V
Vmarker 1 = 0.000 V   Vmarker 2 = 1.200 V

Trigger mode : Edge
On Pos. Edge on Trig3
Trigger Levels
Trig3   = 250.0 mV
Holdoff = 70.000 ns

**Figure A-5a.74AC11373 Passes Stored Data Test on
High Impedance to Low Transition (ZL)**
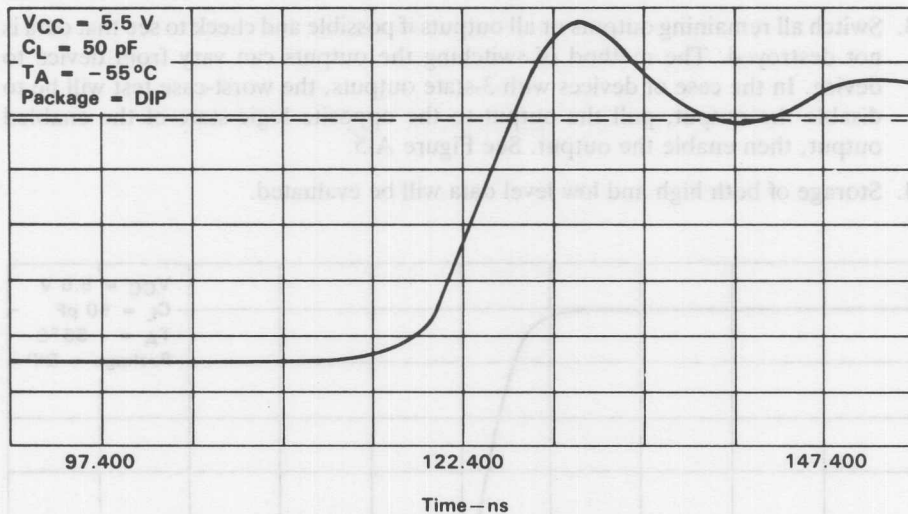
41

V_{CC} = 5.5 V

V_{CC} = 5.5 V
C_L = 50 pF
T_A = −55°C
Package = DIP

97.400   122.400   147.400

Time—ns

CH.2 = 1.000 V/div	Offset = 2.500 V
Timebase = 5.00 ns/div	Delay = 122.400 ns
Delta V = 1.100 V	
Vmarker 1 = 4.400 V	Vmarker 2 = 5.500 V

Trigger mode : Edge
On Pos. Edge on Trig3
Trigger Levels
Trig3 = 2.000 mV
Holdoff = 70.000 ns

**Figure A-5b. 74AC11373 Passes Stored Data Test on the
High Impedance to High Transition (ZH)**

SIMULTANEOUS SWITCHING EVALUATION (MULTIPLE INPUT DEVICES, SINGLE OR COMPLIMENTARY OUTPUTS)

This simultaneous switching test will be used to determine the magnitude of an active output during multiple input switching of devices with a single or single complimentary outputs.

Simultaneous Switching Test Conditions

Input Voltages	Test Conditions	Load Circuit	Test Board
V_{IH} = AC 80% V_{CC} ACT 2.5 V	V_{CC} = 5 V T_A = 25°C and	per data book spec	ESH 300-24 or ESH 300-28
V_{IL} = AC 20% V_{CC} ACT 0.5 V	V_{CC} = 5.5 V T_A = 55°C		

V_{OHV} and V_{OLP} are measured with respect to a ground reference near the output under test. See Figure A-6.

Input pulses have the following characteristics: pulse repetition rate 1 MHz, tr = 3 ns, tf = 3 ns, and skew ≤ 1 ns.

OUTPUT UNDER TEST V_{OLP} ——
V_{OL} ——

V_{OH}
V_{OHV}
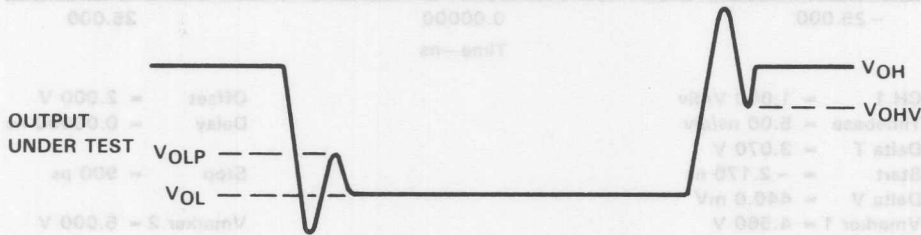
NOTES: A. V_{OHV} and V_{OLP} are measured with respect to ground reference near the output under test.

B. Input pulses have the following characteristics: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 1 ns.

Figure A-6. Dynamic-Output Disturbance Voltage Waveform

Output Low-to-High Disturbance

Switch N-1 inputs with the Nth input held in the appropriate state to obtain a low-to-high transition on the output. See Figure A-7.

V_{CC} = 5 V
C_L = 50 pF
T_A = 25 °C
PACKAGE = DIP

−25.000   0.00000   25.000

Time—ns
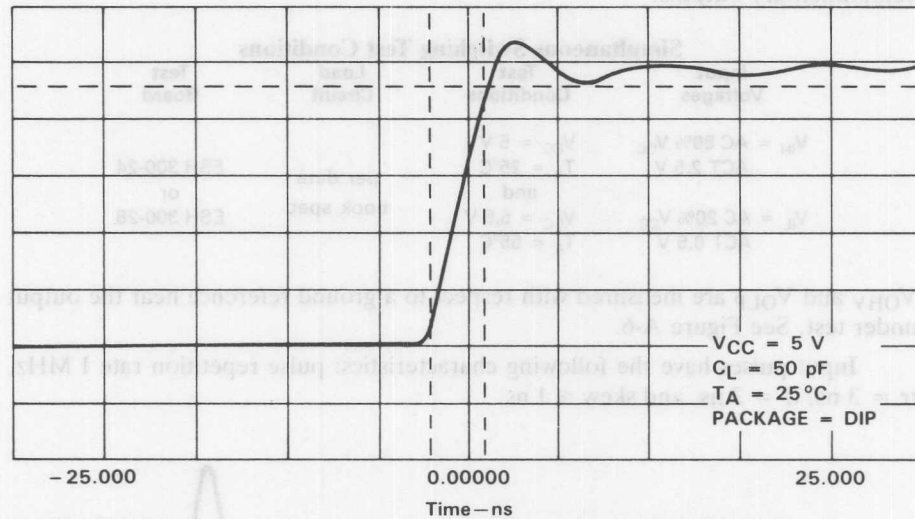
CH.1 = 1.000 V/div	Offset = 2.000 V
Timebase = 5.00 ns/div	Delay = 0.00000 ns
Delta T = 3.070 V	
Start = −2.170 ns	Stop = 900 ps
Delta V = 440.0 mV	
Vmarker 1 = 4.560 V	Vmarker 2 = 5.000 V

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 3.200 V
Holdoff = 70.000 ns

7 INPUTS SWITCHING, 1 HIGH

Figure A-7. Dynamic V_{OHV} Nominal Measurement on 74ACT11030

Output High-to-Low Disturbance

Switch N-1 inputs with the Nth input held in the appropriate state to obtain a high-to-low transition on the output. See Figure A-8.

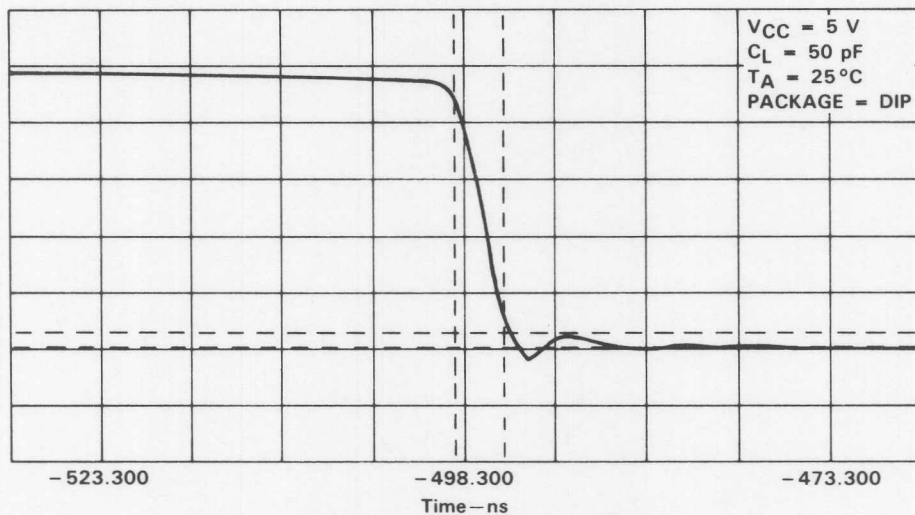|	
CH.1 = 1.000 V/div	Offset = 2.000 V
Timebase = 5.00 ns/div	Delay = −498.300 ns
Delta T = 2.750 ns	
Start = −498.810 ns	Stop = −496.060 ns
Delta V = 280.0 mV	
Vmarker 1 = 0.000 V	Vmarker 2 = 280.0 mV

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 3.200 mV
Holdoff = 70.000 ns

7 INPUTS SWITCHING, 1 HIGH

Figure A-8. Dynamic V_{OLP} Nominal Measurement on 74ACT11030

Output High-to-Low Disturbance

Switch N-1 inputs with the Nth input held in the appropriate state to obtain a high-to-low transition on the output. See Figure A-8.

VCC = 5 V	
C_L = 50 pF	
T_A = 25°C	
PACKAGE = DIP	

Time—ns

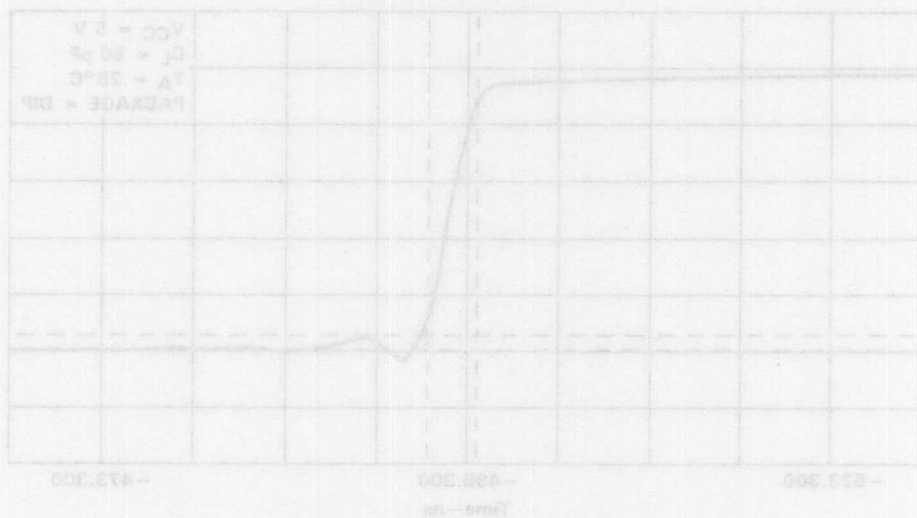|			
CH.1 = 1.000 V/div		Offset = 2.000 V	
Timebase = 5.00 ns/div		Delay = -495.300 ns	
Delta T = 2.750 ns			
Start = -498.810 ns		Stop = -496.060 ns	
Delta V = 280.0 mV			
Vmarker 1 = 0.000 V		Vmarker 2 = 280.0 mV	

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 3.200 mV
Holdoff = 70.000 ns

7 INPUTS SWITCHING, 1 HIGH

Figure A-8. Dynamic V_{OLP} Nominal Measurement on 74ACT11030

Appendix B

ACL Simultaneous Switching Characterization Board Component List

COMPONENT	VENDOR	ORDER NO.
LAB BOARD	ESH INC. 3020 SOUTH PARK DRIVE TEMPE, ARIZONA 85282-3158 (602) 438-1112	LAB-300-24 OR LAB-300-28
0.1 µF DIP CAPACITOR		65F928
AND	NEWARK ELECTRONICS 10727 PLANO ROAD DALLAS, TEXAS 75238 (214) 340-3585	
47 pF CHIP CAPACITOR		81F2006
450 Ω and 50 Ω CHIP RESISTOR	ERIKSON SALES 8350 MEADOW ROAD SUITE 184 DALLAS, TEXAS 75231 (214) 739-5833	ERJ8EKF-4530
NONINSULATED PIN JACKS AND 50 Ω SNAP ON RECEPTACLES AND TERMINATORS	POWELL ELECTRONICS 1933 WESTRIDGE DR. LAS COLINAS, IRVING, TX 75062 (214) 550-0547	006-4820 51-043-0000 61-001-0900

(These terminators are converted to 50 Ω terminators in the lab)

The number of units ordered depends upon the number of outputs and inputs a device may have. All outputs have a 47-pF capacitor and a 450-Ω resistor in parallel between the output and ground. The capacitor is placed on the board as close to the device under test as possible on the opposite side of the board. Any output not terminated with a 50-Ω probe must be terminated with a 50-Ω load. Each input or set of inputs driven by a signal pulse generator must be terminated with a single 50-Ω resistor to ground. A 0.1-μF decoupling capacitor is connected between V_{CC} and ground.